Experiment 09

DC Analysis of Junction Field Effect Transistor (JFET)

Objective:

To understand Junction Field Effect Transistor (JFET) and its output characteristics.

Introduction:

The Junction Field Effect Transistor, or JFET, is a voltage controlled three terminal unipolar semiconductor device available in N-channel and P-channel configurations In the *Bipolar Junction Transistor* topic, we saw that the output Collector current of the transistor is proportional to input current flowing into the Base terminal of the device, thereby making the

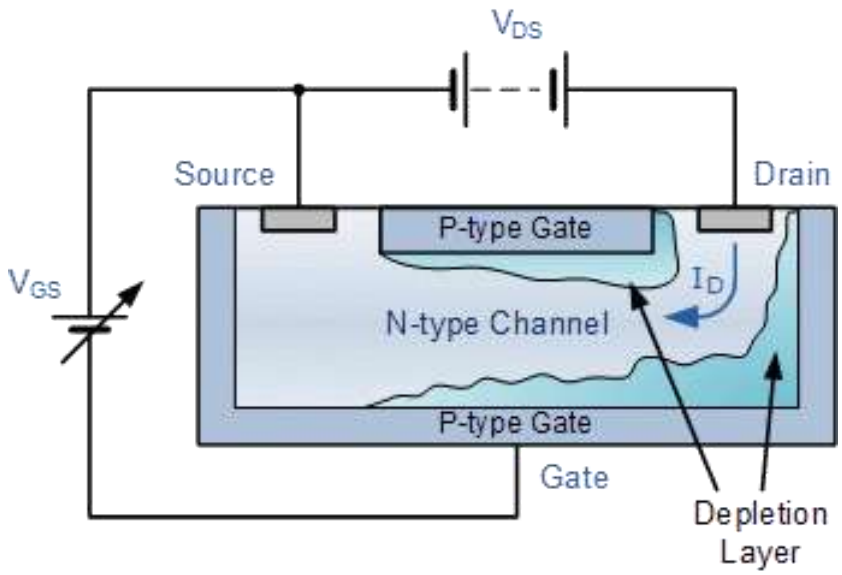


Figure 1

11.1: N-Channel JFET

bipolar transistor a "CURRENT" operated device (Beta model) as a smaller current can be used to switch a larger load current. The **Field Effect Transistor**, or simply **FET** however, uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the **Field Effect Transistor** a "VOLTAGE" operated device.

The **Field Effect Transistor** is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterparts. For example, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit

Figure 11.2: Typical Field Effect Transistor

applications to replace their equivalent bipolar junction transistors (BJT) cousins. The **Junction Field Effect Transistor** (JFET) has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively. JFET is an essential component for precision level voltage operated controls in analog electronics. We can use JFET as voltage-controlled resistors or as a switch, or even make an amplifier using the JFET. It is also an energy efficient version to replace the BJTs. JFET provides low power consumption and fairly low power dissipations, thus improving the overall efficiency of the circuit. It also provides very high input impedance which is a major advantage over a BJTs.

Basic Types of JFET

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

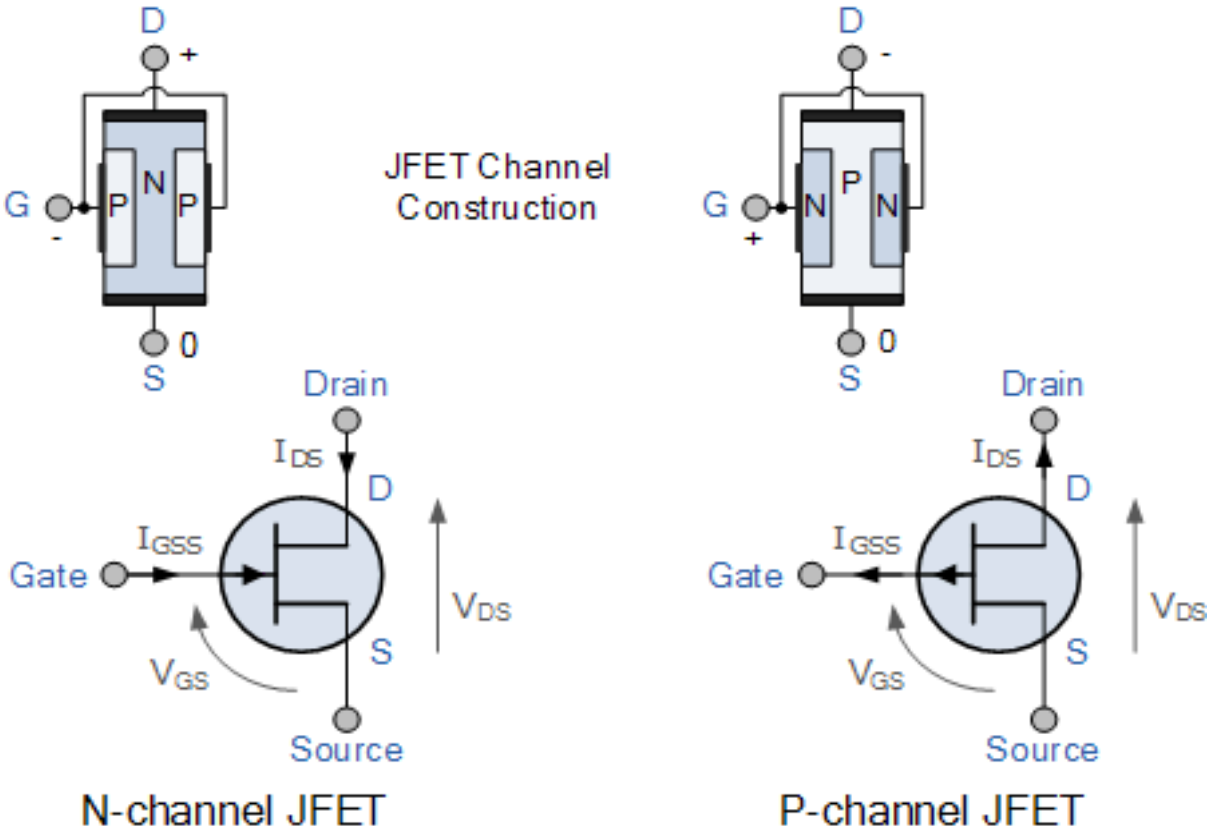
Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a more efficient conductor compared to their P-channel counterparts. We have said previously that there are two ohmic electrical connections at either end of the channel called the Drain and the Source. But within this channel there is a third

electrical connection which is called the Gate terminal and this can also be a P-type or N-type material forming a PN-junction with the main channel. The relationship between the connections of a junction field effect transistor and a bipolar junction transistor are compared below.

Comparison of Connections between a JFET and a BJT

Bipolar Junction Transistor (BJT)	Field Effect Transistor (FET)
Emitter (E) >> Source (S)	
Base (B) >> Gate (G)	
Collector (C) >> Drain (D)	

The symbols and basic construction for both configurations of JFETs are shown below.

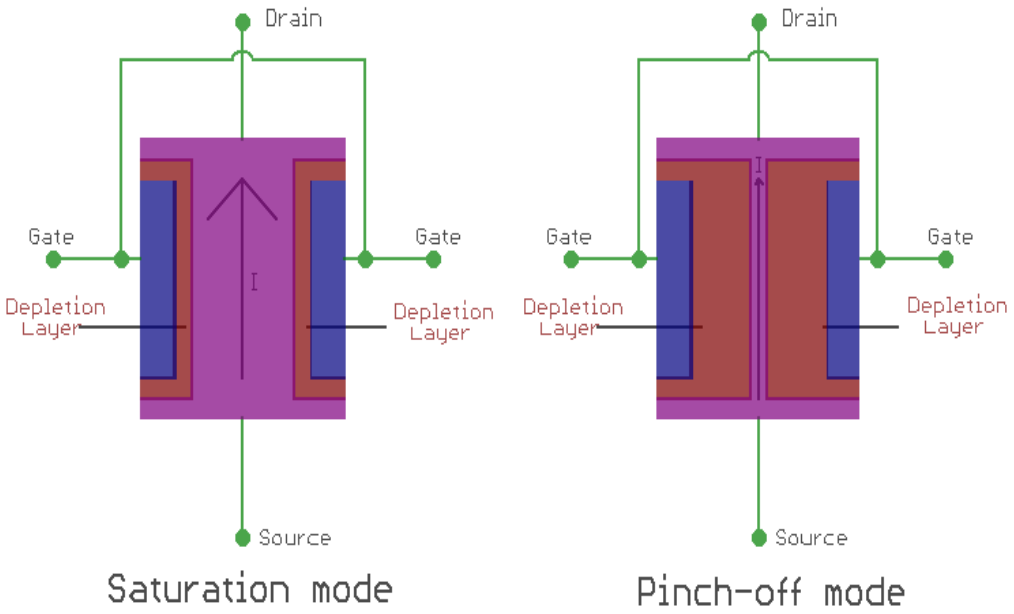


The semiconductor "channel" of the **Junction Field Effect Transistor** is a resistive path through which a voltage V_{DS} causes a current I_D to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.

The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a “depletion layer” to be formed within the channel and whose width increases with the bias. The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive. The main difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Working of JFET

One best example to understand the working of a JFET is to imagine the garden hose pipe. Suppose a garden hose is providing a water flow through it. If we squeeze the hose the water flow will be less and at a certain point if we squeeze it completely there will be zero water flow. JFET works exactly in that way. If we interchange the hose with a JFET and the water flow with a current and then construct the current-carrying channel, we could control the current flow. When there is no voltage across gate and source, the channel becomes a smooth path which is wide open for electrons to flow. But the reverse thing happens when a voltage is applied between gate and source in reverse polarity, that makes the P-N junction reversed



biased and makes the channel narrower by increasing the depletion layer and could put the JFET in cut-off or pinch off region.

In the below image we can see the **saturation mode and pinch off mode** and we will be able to understand the **depletion layer became wider and the current flow becomes less**.

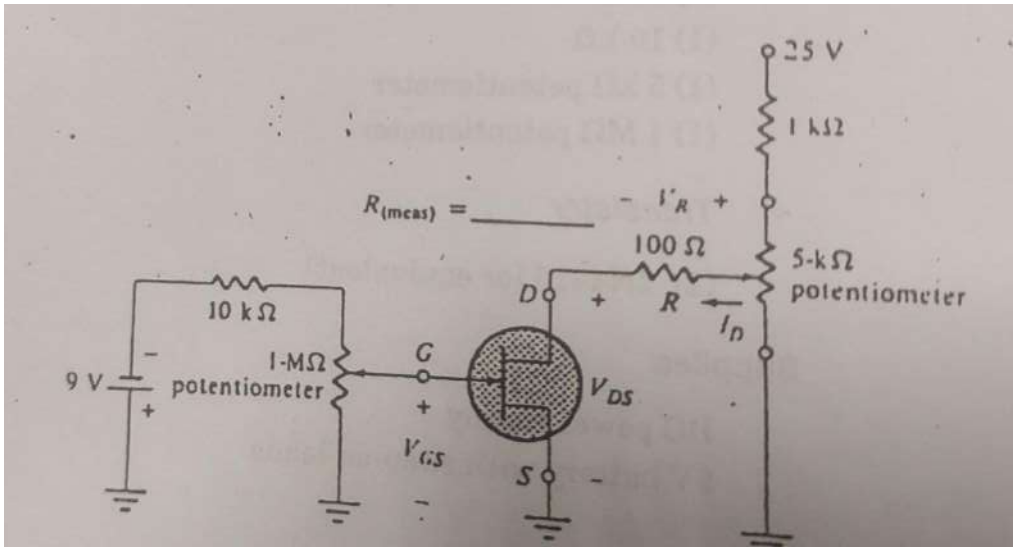
If we want to switch off a JFET we need to provide a negative gate to source voltage denoted as V_{GS} for an N-type JFET. For a P-type JFET, we need to provide positive V_{GS}.

JFET only works in the depletion mode, whereas MOSFETs have depletion mode and enhancement mode.

Lab Activity:

Task: 1

Construct the network as shown below using 2N4416. Insert the measured value of R.



Task: 2

Vary the 1MΩ potentiometer until VGS =0V. Recall that ID=IDSS when VGS = 0V. Set VDS to 8V by varying the 5KΩ potentiometer. Measure the Voltage VR.

VR=

Calculate the saturation Current from IDSS = ID = VR/R using the measured resistance value.

IDSS =

Task: 3

Maintain VDS at about 8V and reduce VGS until VR drops to 1mV at this level ID = VR/R =~0A compared to typical operating levels. Recalls that Vp is the voltage VGS that results in Id = 0mA. Record the pich off voltage below:

Vp =

Task: 4

Using the determined values of IDSS and Vp, find Id for VGS = 5V.

$$ID = IDSS \times (1 - \frac{VGS}{Vp})^2$$

$$ID =$$

Task: 5

This part of the experiment will determine the ID versus VDS characteristics for an n channel JFET.

a) Using the network use in task 1, vary the two potentiometers until VGS =0V and VDS = 0V. Determine ID from ID= VR/R using the measured value of R and Record in Table 11.1

b) Maintain VGS at 0V and increase VDS through 14V (in 1V steps) and record the calculated values of ID.

c) Vary the 1MΩ potentiometer until VGS =-1V. Maintaining VGS at this level vary VDS through the level of table and record the readings.

d) Plot the

Table 11.1 JFET characteristics table

VGS (V)	**0**	**-1**	**-2**	**-3**	**-4**	**-5**
VDS (V)	**ID (mA)**	**ID (mA)**	**ID (mA)**	**ID (mA)**	**ID (mA)**	**ID (mA)**
0						
1						
2						
3						

4						
5						
6						
7						
8						
9						
10						
11						
12						
13						

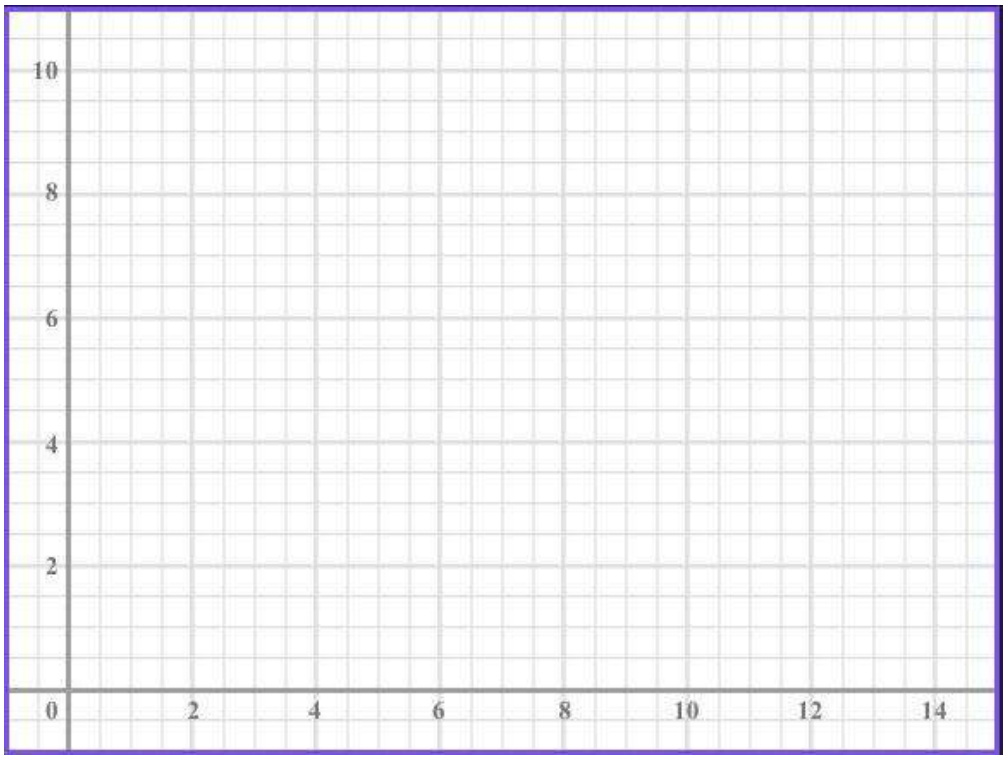


Figure 1 Transfer Characteristics of 2N4416

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge related to DC Analysis of Junction Field Effect Transistor (JFET)	Makes few critical errors in applying procedural knowledge related to DC Analysis of Junction Field Effect Transistor (JFET)	Makes some non-critical errors in applying procedural knowledge related to DC Analysis of Junction Field Effect Transistor (JFET)	Applies the procedural knowledge in perfect ways related to DC Analysis of Junction Field Effect Transistor (JFET)	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**