Experiment No 3

Familiarization with Logic Gates and Truth Table based Verification

3.1 Objectives

After completing this experiment, student will be able to:

- Comprehend different types of logic gates used in digital logic
- Determine experimentally the truth tables of basic logic gates like NOT, AND, OR, NAND and NOR gates.
- Construct circuits consisting of basic logic gates
- Comprehend different logic families and their characteristics
- Perform truth table based verification

3.2 Background Theory

Logic deals with only two normal conditions: logic "1" or logic "0." These conditions are like the yes or no answers to a question. Either a switch is closed (1) or it isn't (0); either an event has occurred (1) or it hasn't (0); and so on. In Boolean logic, 1 and 0 represent conditions. In positive logic, 1 is represented by the term HIGH and 0 is represented by the term LOW. In positive logic, the more positive voltage is 1 and the less positive voltage is 0. Thus, for positive TTL logic, a voltage of +2.4 V = 1 and a voltage of +0.4 V = 0.

In some systems, this definition is reversed. With negative logic, the more positive voltage is 0 and the less positive voltage is 1. Thus, for negative TTL logic, a voltage of +0.4 V = 1 and a voltage of +2.4 V = 0. Negative logic is sometimes used for emphasizing an active logic level.

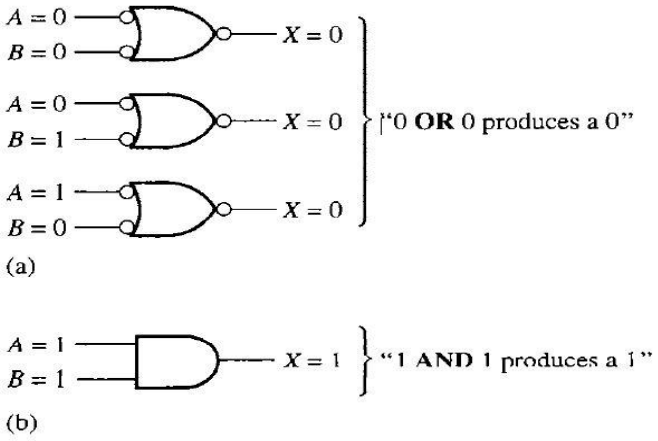


Figure 3.1: Two distinctive shape symbols for an AND gate.

For all of the basic gates, there is a traditional symbol that is used for positive logic and an

alternate symbol for negative logic. For example, an AND gate can be shown in negative logic with an OR symbol and "inverting bubbles" on the input and output, as illustrated with the three symbols in Figure 3.1 (a). This logic can be read as "If A or B is LOW, the output is LOW." The exact same gate can be drawn as in Figure 3.1 (b), where it is now shown as a traditional active-HIGH gate and read as "If both A and B are HIGH, the output is HIGH." The different drawings merely emphasize one or the other of the following two rules for an AND gate:

- Rule 1: If A is LOW or B is LOW or both are LOW, then X is LOW.
- Rule 2: If A is HIGH and B is HIGH, then X is HIGH.

The operation can also be shown by the truth table. The AND truth table is:

Table 3.1: Truth table

Inputs		Outputs
A	B	X
LOW	LOW	
LOW	HIGH	
HIGH	LOW	
HIGH	HIGH	

Notice that the first rule describes the first three lines of the truth table and the second rule describes the last line of the truth table. Although two rules are needed to specify completely the operation of the gate, each of the equivalent symbols best illustrates only one of the rules. If you are reading the symbol for a gate, read a bubble as a logic 0 and the absence of a bubble as a logic 1. The first three lines of the truth table are illustrated with the negative-logic OR symbol (Figure 3.1 (a)); the last line of the truth table is illustrated with the positive-logic AND symbol (Figure 3.1 (b)). Similar rules and logic diagrams can be written for the other basic gates. A useful method of dealing with negative logic is to label the signal function with a bar written over the label to indicate that the signal is LOW when the stated condition is true.

3.2.1 Overview of Logic gates

The symbols for the basic logic gates are shown in Figure 3.2. The newer ANSI/IEEE rectangular symbols are shown along with the older distinctive- shape symbols. The ANSI/IEEE symbols contain a qualifying symbol to indicate the type of logic operation performed. The distinctive-shape symbols for logic gates are still very popular because they enable you to visualize the standard Boolean operations of AND, OR, and INVERT immediately. The distinctive shapes also enable you to analyze logic networks because each gate can be represented with a positive logic symbol or an equivalent negative logic symbol. Both shapes are used in this experiment. In addition to the AND, OR, and INVERT functions, two other basic gates are very important to logic designers. These are the NAND and NOR gates, in which the output of AND and OR, respectively, have been negated. These gates are

important because of their "universal" property; they can be used to synthesize the other Boolean logic functions including AND, OR, and INVERT functions. Two gates that are sometimes classified with the basic gates are the exclusive-OR (abbreviated XOR) and the exclusive-NOR (abbreviated XNOR) gates. These gates always have two inputs. The symbols are shown in Figure 3.2 (f) and (g). The output of the XOR gate is HIGH when either A or B is HIGH, but not both (inputs "disagree"). The XNOR is just the opposite; the output is HIGH only when the inputs are the same (agree). For this reason, the XNOR gate is sometimes called a COINCIDENCE gate.

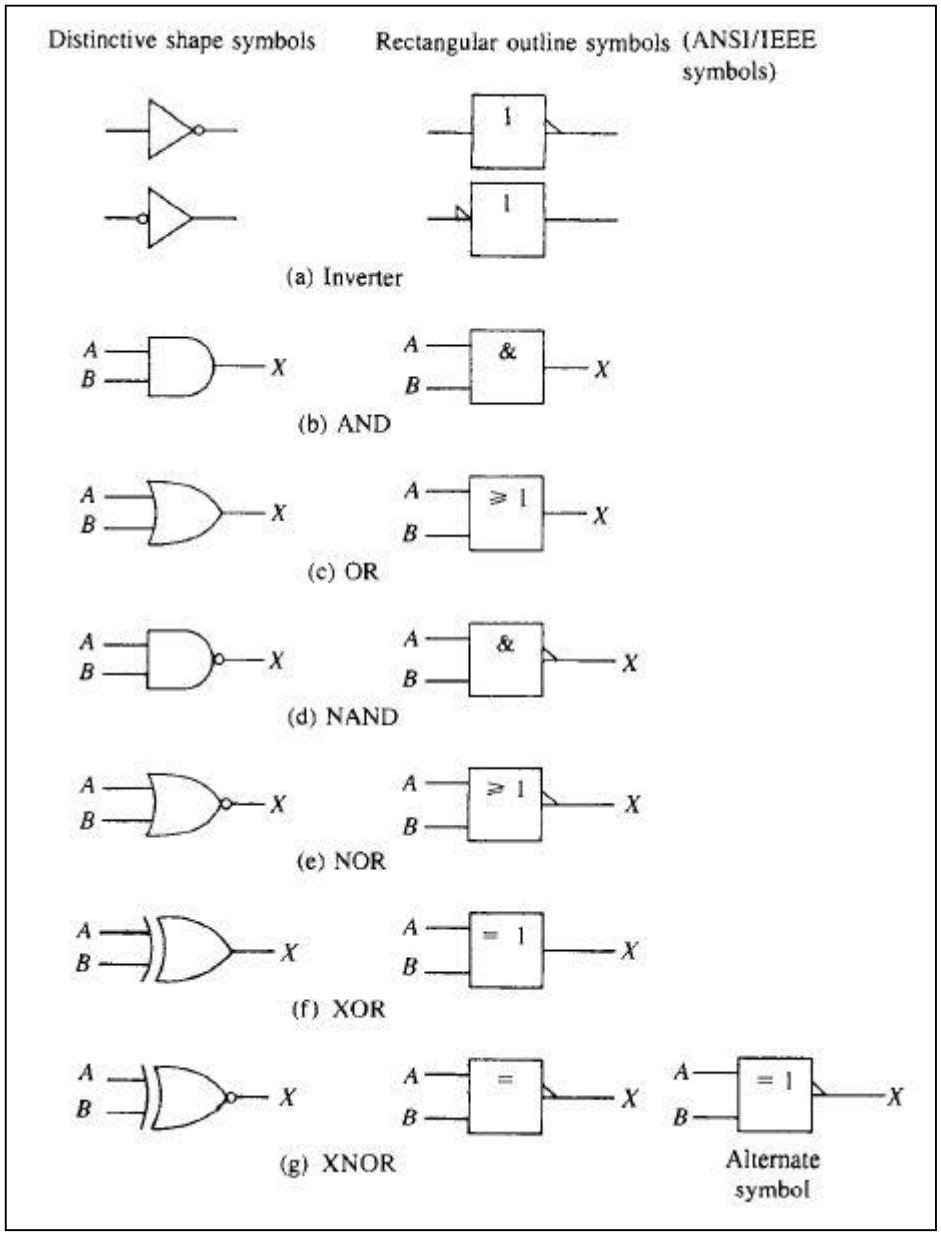


Figure 3.2: Symbols of Basic Logic Gates

3.2.2 Classification of Integrated Circuits

3.2.2.1 Small Scale Integration or (SSI)

The first integrated circuits contained only a few transistors and so were called “Small-Scale Integration (SSI). SSI contain up to 10 transistors or a few gates within a single package such as AND, OR, NOT gates. They were very crucial in development of early computers.

3.2.2.2 Medium Scale Integration or (MSI)

SSI was followed by introduction of the devices which contain between 10 and 100 transistors or tens of gates within a single package and perform digital operations such as adders, decoders, counters, flip-flops and multiplexers, so were called “Medium-Scale Integration (MSI).

3.2.2.3 Large Scale Integration or (LSI)

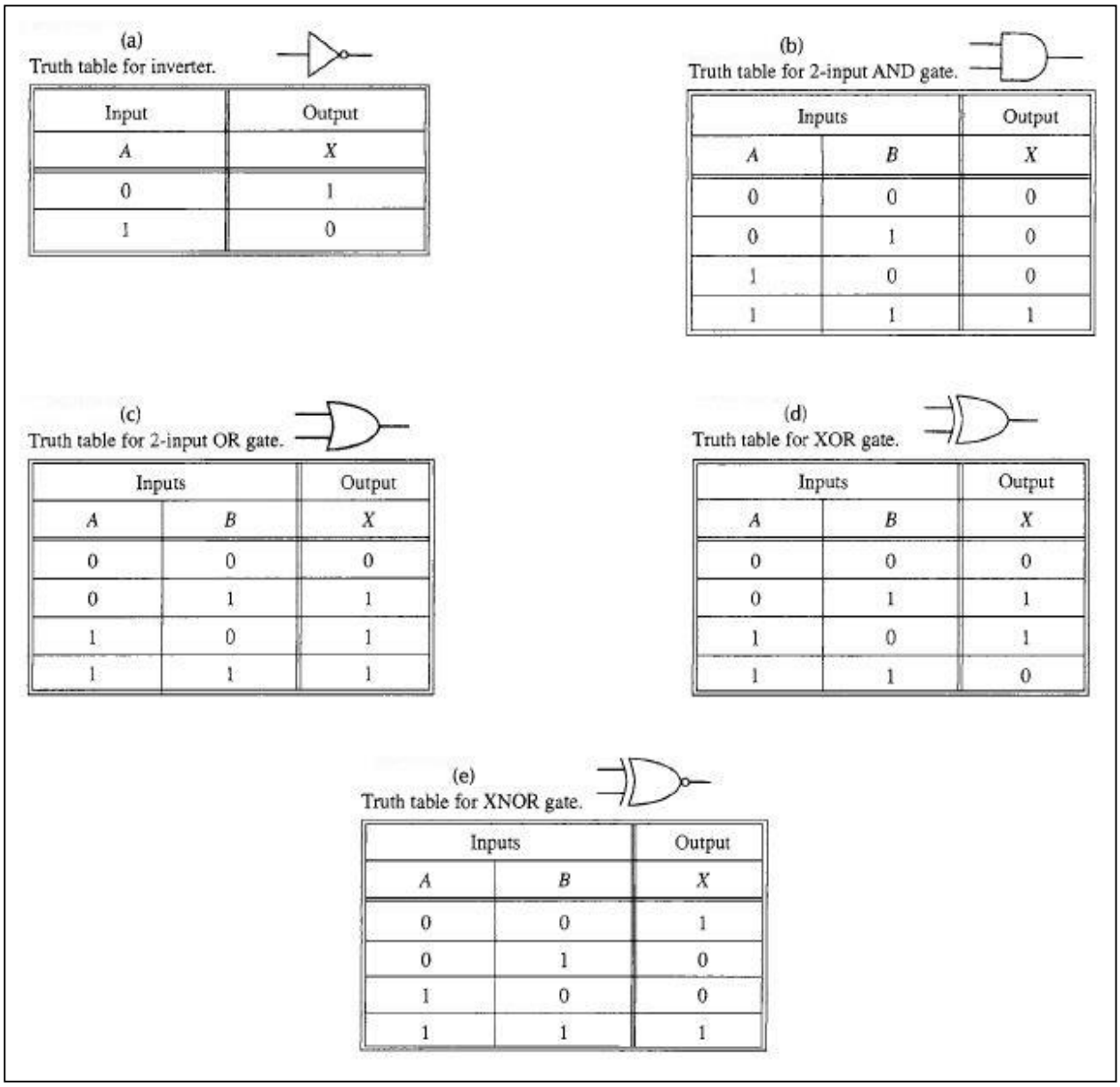
Next development was of Large Scale Integration (LSI). The development of LSI was driven by economic factors and each chip comprised tens of thousands of transistors. It was in 1970s, when LSI started getting manufactured in huge quantities. LSI contains between 100 and 1,000 transistors or hundreds of gates and perform specific digital operations such as I/O chips, memory, arithmetic and logic units.

3.2.2.4 Very-Large Scale Integration or (VLSI)

LSI was followed by Very Large Scale Integration (VLSI) where hundreds of thousands of transistors were used and still being developed. It was for the first time that a CPU was fabricated on a single integrated circuit, to create a microprocessor. In 1986, with the introduction of first one megabit RAM chips, more than one million transistors were integrated. VLSI contains between 1,000 and 10,000 transistors or thousands of gates and perform computational operations such as processors, large memory arrays and programmable logic devices.

3.2.3 Truth Table

The logical operation of any gate can be summarized with a truth table, which shows all the possible inputs and outputs. The truth tables for INVERT, AND, OR, XOR, and XNOR are shown in Figure 3.3(a) through (e). The tables are shown with 1 and 0 to represent positive logic HIGH and LOW, respectively. Except in Figure 3.1(a) (where negative logic is illustrated), only positive logic is used in this lab book and 1 and 0 mean HIGH and LOW, respectively. In this experiment, you will test the truth tables for NAND and NOR gates as well as those for several combinations of these gates. Keep in mind that if any two truth tables are identical, then the logic circuits that they represent are equivalent. In the Further Investigation, look for this idea of equivalence between a 4-gate circuit and a simpler 1-gate equivalent.



(a)
Truth table for inverter.

Input	Output
A	X
0	1
1	0

(b)
Truth table for 2-input AND gate.

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(c)
Truth table for 2-input OR gate.

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

(d)
Truth table for XOR gate.

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

(e)
Truth table for XNOR gate.

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Figure 3.3: Truth tables of Logic gates

3.2.4 Overview of Logic Families

A logic family is a circuit technology that can be used to create many different types of gates: inverter, NAND, NOR, etc.

3.2.4.1 Transistor-Transistor Logic (TTL)

The Transistor-Transistor Logic (TTL) is a logic family made up of BJTs (bipolar junction transistors). As the name suggests, the transistor performs two functions like logic as well as amplifying. The best examples of TTL are logic gates namely the 7402 NOR Gate & the 7400

NAND gate. TTL logic includes several transistors that have several emitters as well as several inputs. The types of TTL or transistor-transistor logic mainly include Standard TTL, Fast TTL, Schottky TTL, High power TTL, Low power TTL & Advanced Schottky TTL. The designing of TTL logic gates can be done with resistors and BJTs. There are several variants of TTL which are developed for different purposes such as the radiation-hardened TTL packages for space applications and Low power Schottky diodes that can provide an excellent combination of speed and lesser power consumption.

3.2.4.1.1 Classification of Transistor-Transistor Logic

It is a logical family consisting completely of transistors. It employs a transistor with multiple emitters. Commercially it starts with the 74 series like the 7404, 74S86, etc. TTLs are classified based on the output.

3.2.4.1.2 TTL Family Features

The features of the TTL family include the following:

- Logic low level is at 0 or 0.2V.
- Logic high level is at 5V.
- Typical fan out of 10. It means it can support at most 10 gates at its output.
- A basic TTL device draws a power of almost 10mW, which reduces with the use of Schottky devices.
- The average propagation delay is about 9ns.
- The noise margin is about 0.4V.

3.2.4.2 Complementary Metal Oxide Semiconductor (CMOS)

The term CMOS stands for "Complementary Metal Oxide Semiconductor". This is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs, and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs).

The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide

Semiconductor transistor consists of P-channel MOS (PMOS) and N-channel MOS (NMOS). Please refer to the link to know more about the fabrication process of CMOS transistor.

3.2.4.2.1 CMOS Family Features

- CMOS supports a very large fan-out, more than 50 transistors.
- It has excellent noise immunity amongst all families.
- A logic low voltage for CMOS is about
- A logic high voltage for ECL is somewhere between 4.5V to 5V.
- The propagation delay is the worst when compared with TTL and ECL families at about 200ns.

3.2.4.3 Emitter Coupled Logic (ECL)

ECL families use overdriven BJT differential amplifiers with single-ended inputs. The emitters of the transistors are connected all together, hence the name 'emitter-coupled' logic families. The transistors in this system never saturate; their logic high and logic low levels are chosen close to one another, thus eliminating the possibility of saturation in the transistors. The transistors are thus operated in the active region or the cut-off region.

These transistors use the property of current switching. Thus this family is also known as Current Steering Logic (CSL) or Current Mode Logic Families (CML). It makes use of a transistor-based differential amplifier to amplify and combine digital signals. The transistors are differential amplifiers, with their emitters coupled. Cryptographic applications and high-speed requirements use ECL Logic.

3.2.4.3.1 ECL Family Features

- The output of an ECL system has a very low impedance, thus having a fan-out of about 25.
- The propagation time is about 1ns, making it the fastest logic family.
- A logic low voltage for ECL is about -1.7V to -1.75V.
- A logic high voltage for ECL is about -0.8V.
- It is the fastest amongst all the logic families.
- It has an average propagation delay time of about 1ns-4ns.

3.2.5 Characteristics of Logic Families

The main characteristics of Logic families include:

- Propagation delay
- Fan-in
- Fan-out
- Noise Immunity
- Power Dissipation

3.2.5.1 Propagation delay

Propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change.

3.2.5.2 Fan-in

It determines the number of inputs the logic gate can handle.

3.2.5.3 Fan-out

Determines the number of circuits that a gate can drive.

3.2.5.4 Noise-Immunity

Maximum noise that a circuit can withstand without affecting the output.

3.2.5.5 Power

When a circuit switches from one state to the other, power dissipates.

3.3 Lab Activities

3.3.1 Task-1: Truth table verification of basic logic gates

Verify and fill the truth tables of the logic gates given below by constructing their circuits on breadboard. Show the outputs to your instructor.

Table 3.2: NOT Gate Truth table

Input1	Output
A	X
0	
0	
1	
1	

Table 3.3: AND Gate Truth table

Inputs		Output
A	B	X
0	0	
0	1	
1	0	
1	1	

Table 3.4: OR Gate Truth table

Inputs		Output
A	B	X
0	0	
0	1	
1	0	
1	1	

Table 3.5: NAND Gate Truth table

Inputs		Output
A	B	X
0	0	
0	1	
1	0	
1	1	

Table 3.6: NOR Gate Truth table

Inputs		Output
A	B	X
0	0	
0	1	
1	0	
1	1	

3.3.2 Task-2

Construct the given circuits on breadboard and fill the tables given below.

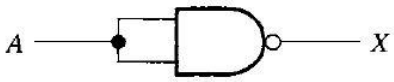


Figure 3.4

Table 3.7: Truth table for Figure 3.4

Input	Output	Measured Output Voltage
A	X	
0		
0		
1		
1		

3.3.3 Task-3

a) Construct the given circuits on breadboard and fill the tables given below.

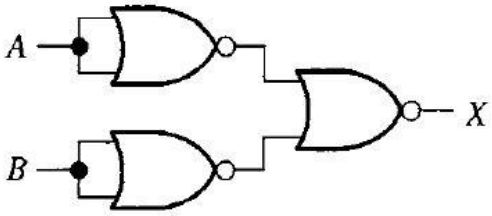


Figure 3.5

Table 3.8: Truth table for Figure 3.5

Input	Output	Measured Output Voltage
A	X	
0		
0		
1		
1		

b) Construct the given circuits on breadboard and fill the tables given below.

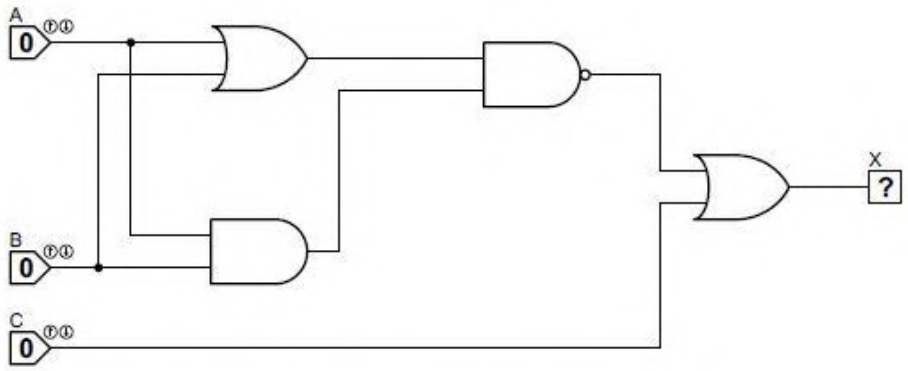


Figure 3.6

Table 3.9: Truth table for Figure 3.6

Inputs			Output	Measured Output Voltage
A	B	C	X	
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge of logic gates	Makes few critical errors in applying procedural knowledge of logic gates	Makes some non-critical errors in applying procedural knowledge of logic gates	Applies the procedural knowledge of logic gates in perfect ways	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**