Experiment No 9

Finite state machine (FSM) based design of Sequential Circuits

9.1 Objectives:

After completing this experiment, student will be able to:

- Describe Graphical representation of sequential circuit.
- Describe the different types of Finite state machine.
- Design a sequential circuit from state diagram.

9.2 Background Theory

We know that synchronous sequential circuit's change affect their states for every positive or negative transition of the clock signal based on the input. So, this behavior of synchronous sequential circuits can be represented in the graphical form and it is known as state diagram. A synchronous sequential circuit is also called as Finite State Machine FSM, if it has finite number of states. There are two types of FSMs:

- Mealy State Machine
- Moore State Machine

9.2.1 Mealy State Machine

A Finite State Machine is said to be Mealy state machine, if outputs depend on both present inputs & present states. The block diagram of Mealy state machine is shown in the following figure.

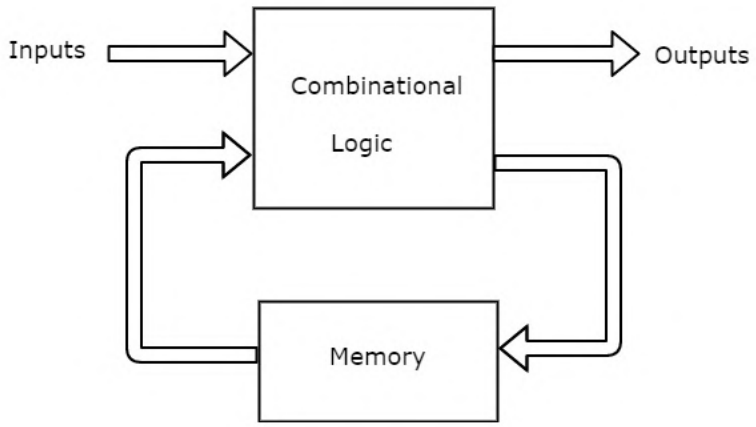


Figure 9.1 Block Diagram of Mealy State Machine.

As shown in figure 9.1, there are two parts present in Mealy state machine. Those are combinational logic and memory. Memory is useful to provide some or part of previous outputs present states as inputs of combinational logic. So, based on the present inputs and present states, the Mealy state machine produces outputs. Therefore, the outputs will be valid only at

positive or negative transition of the clock signal. The state diagram of Mealy state machine is shown in the following figure.

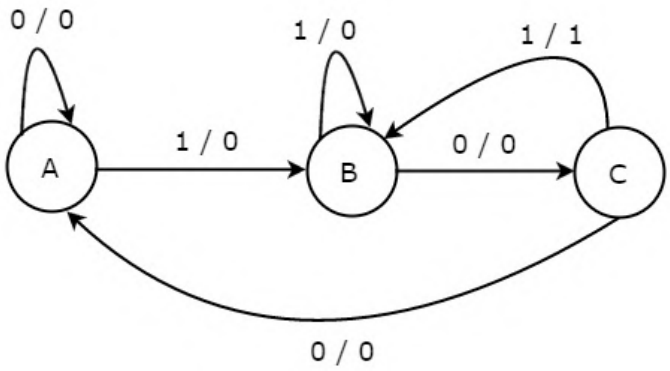


Figure 9.2 State Diagram of Mealy State Machine

In the above figure, there are three states, namely A, B & C. These states are labelled inside the circles & each circle corresponds to one state. Transitions between these states are represented with directed lines. Here, 0 / 0, 1 / 0 & 1 / 1 denotes input / output. In the above figure, there are two transitions from each state based on the value of input, x. In general, the number of states required in Mealy state machine is less than or equal to the number of states required in Moore state machine. There is an equivalent Moore state machine for each Mealy state machine.

9.2.2 Moore State Machine

A Finite State Machine is said to be Moore state machine, if outputs depend only on present states. The block diagram of Moore state machine is shown in the following figure.

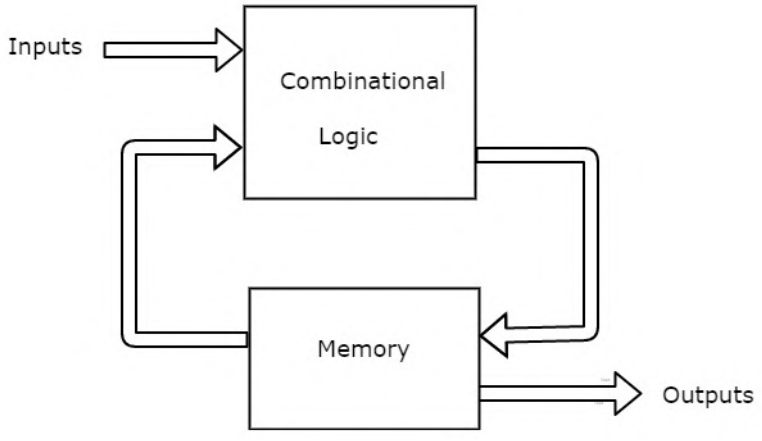


Figure 9.3 Block Diagram of Moore State Machine

As shown in figure 9.3, there are two parts present in Moore state machine. Those are combinational logic and memory. In this case, the present inputs and present states determine the next states. So, based on next states, Moore state machine produces the outputs. Therefore,

the outputs will be valid only after transition of the state. The state diagram of Moore state machine is shown in the following figure.

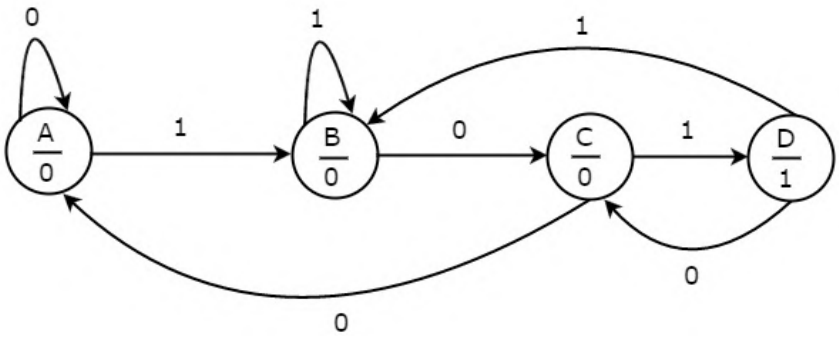


Figure 9.4 State Diagram of Moore State Machine

In the above figure, there are four states, namely A, B, C & D. These states and the respective outputs are labelled inside the circles. Here, only the input value is labeled on each transition. In the above figure, there are two transitions from each state based on the value of input, x. In general, the number of states required in Moore state machine is more than or equal to the number of states required in Mealy state machine. There is an equivalent Mealy state machine for each Moore state machine. So, based on the requirement we can use one of them.

9.3 State Diagram

State Diagram is graphical representation of the state table. In State Diagram, States are represented using circles and transition between states is represented using directed lines connecting the states. Directed lines are labeled with Input/output pair.

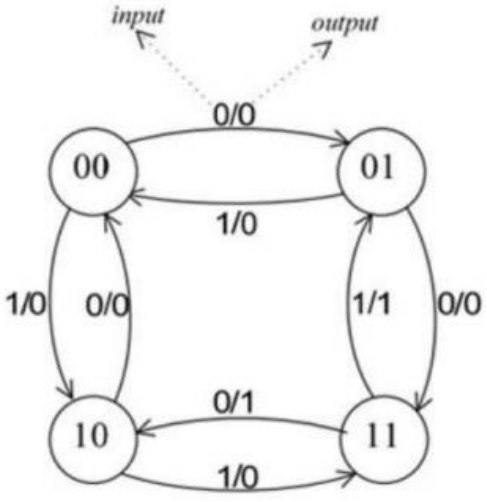
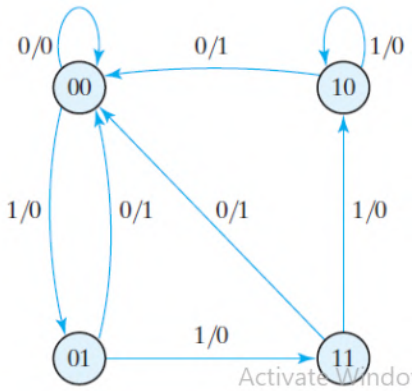


Figure 9.5 Sampled State Diagram

- State Diagram from the state Table

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0



The state diagram provides the same information as the state table. The binary number inside each circle identifies the state of flip-flops. The directed lines are labeled with two binary numbers separated by a slash. The input value during the present state is labeled first and the number after the slash gives the output during the present state.

9.4 Characteristic and Excitation Tables of flip-flop

The analysis of a sequential circuit with flip-flops other than the D type is complicated because the relationship between the inputs of the flip-flop and the next stage is not straightforward. This relationship is best described by means of a characteristic table and Excitation table rather than a state equation. The characteristic tables of four flip-flops are shown below:

Table: 1 Flip-Flop Characteristic tables

JK Flip-Flop

J	K	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

RS Flip-Flop

S	R	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Unpredictable

D Flip-Flop

D	$Q(t+1)$	
0	0	Reset
1	1	Set

T Flip-Flop

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

The characteristic table is useful for analysis and for defining the operation of the flip-flop. It specifies the next state when the inputs and present state are known. During the design process, we usually know the transition from present state to next state and wish to find the flip flop

input conditions that will cause the required transition. For this reason, we need a table that lists the required inputs for a given change of state. Such a list is called an excitation table.

Table: 2 Flip-Flops Excitation tables

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T flip-flop

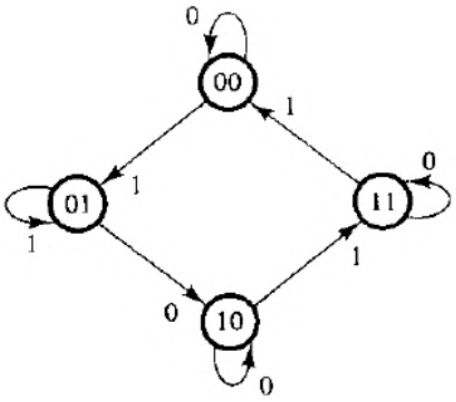
Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

9.5 Design Procedure

Design of a clocked sequential circuit starts from a set of specifications and culminates in a logic diagram or a list of Boolean functions from which the logic diagram can be obtained. Design procedure consists of choosing the flip-flops and finding the required combinational logic. Number of flip-flops is determined from the number of states required. Any type of F/F can be used in design procedure. JK F/F's are preferred for general applications, D F/F for data transfer and T F/F for counters. Flowing steps should be followed while designing sequential circuit.

- From Design Specifications derive a state diagram
- Obtain an Excitation Table showing state transition and F/F inputs
- Use K-Maps to get simplified F/F input equations and output equations
- Draw the logic diagram of sequential circuit

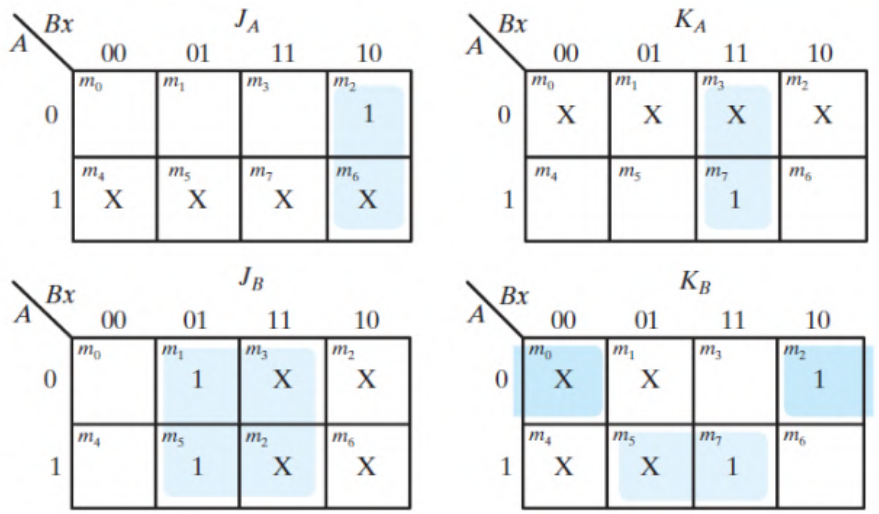
e.g. **Design a sequential circuit using JK Flip Flops for the following state diagram**



Step: 1 Conversion of State Diagram into Excitation Table

Present State		Input	Next State		Flip-Flop Inputs			
A	**B**	**x**	**A**	**B**	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

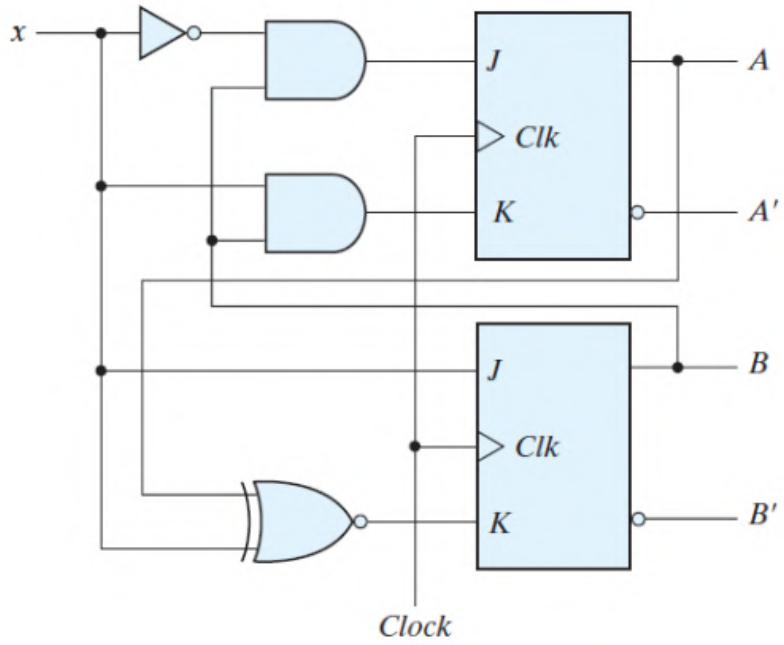
Step: 2 Simplified Combinational Logic for Flip Flop Inputs



$$J_A = Bx' \qquad K_A = Bx$$

$$J_B = x \qquad K_B = (A \oplus x)'$$

Step: 3 Logic Diagram of Sequential Circuit



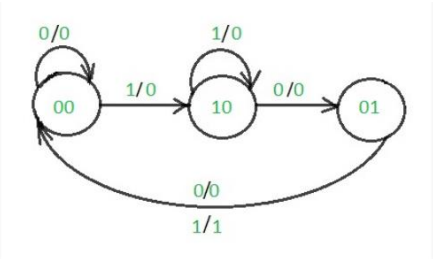
$$J_A = Bx'$$
$$K_A = Bx$$
$$J_B = x$$
$$K_B = (A \oplus x)'$$

Figure 9.6 Logic Diagram of sequential circuit

9.6 Lab Activities

9.6.1 Task-1:

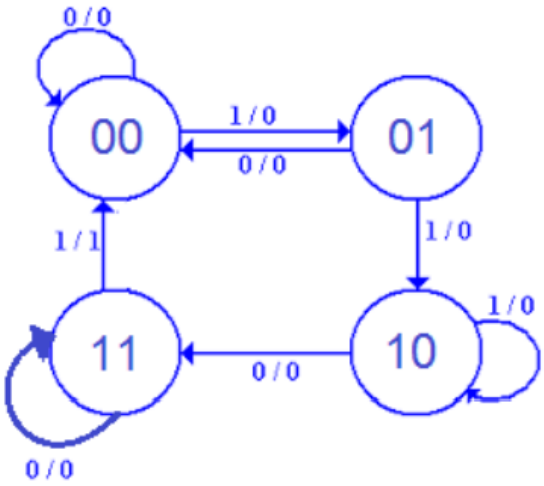
Design and Implement a Sequence Detector using J-K flip-flops. FSM of a sequence detector is shown below:



FSM of Sequence detector

9.6.2 Task-2:

Design and Implement following sequential circuit using D Flip Flop.



Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge of (FSM) based design of Sequential Circuits	Makes few critical errors in applying procedural knowledge of (FSM) based design of Sequential Circuits	Makes some non-critical errors in applying procedural knowledge of (FSM) based design of Sequential Circuits	Applies the procedural knowledge of (FSM) based design of Sequential Circuits in perfect ways	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**