Experiment No 5

Combinational Circuits Implementation using K-Maps

5.1 Objectives:

After completing this experiment, student will be able to:

- Use a Karnaugh map to simplify the expression.
- Use don’t care condition in K-Map based simplification.
- Design a logic circuit based on K-Map.
- Build and test a circuit that implements the simplified expression.

5.2 Background Theory

A combinational circuit is the digital logic circuit in which the output depends on the combination of inputs at that point of time with total disregard to the past state of the inputs. The digital logic gate is the building block of combinational circuits. The function implemented by combinational circuit is depend upon the Boolean expressions. On the other hand, sequential logic circuits, consists of both logic gates and memory elements such as flip-flops. Figure 5.1 below shows the combinational circuit having n inputs and m outputs. The n number of inputs shows that there are 2^n possible combinations of bits at the input. Therefore, the output is expressed in terms m Boolean expressions.

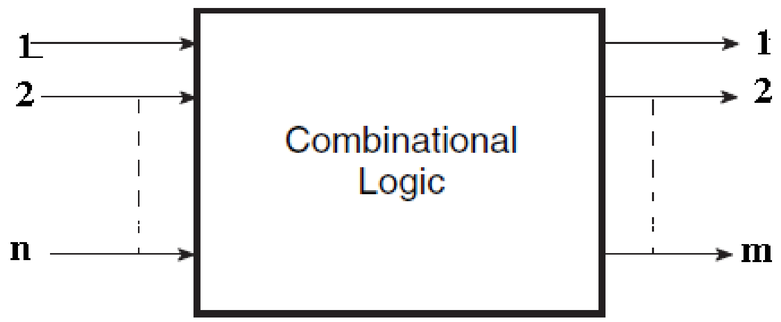


Figure 5.1: Combinational Circuit

Karnaugh maps or K-maps for short provide another means of simplifying and optimizing logical expressions. This is a graphical technique that utilizes a sum of product (SOP) form. SOP forms combine terms that have been ANDed together that then get ORed together. This format lends itself to the use of De Morgan's law which allows the final result to be built with only NAND gates. The K-map is best used with logical functions with four or less input variables. One of the advantages of using K-maps for reduction is that it is easier to see when a circuit has been fully simplified. Another advantage is that using K-maps leads to a more structured process for minimization.

In order to use a K-map, the truth table for a logical expression is transferred to a K-map grid. The grid for two, three, and four input expressions are shown in figure 5.1. Each cell corresponds to one row in a truth table or one given state in the logical expression. The order of the items in the grid is not random at all; they are set so that any adjacent cell differs in value by the change in only one variable. Because of this, items can be grouped together easily in rectangular blocks of two, four, and eight to find the minimal number of groupings that can cover the entire expression. Note that diagonal cells require that the value of more than two inputs change, and that they also do not form rectangles.

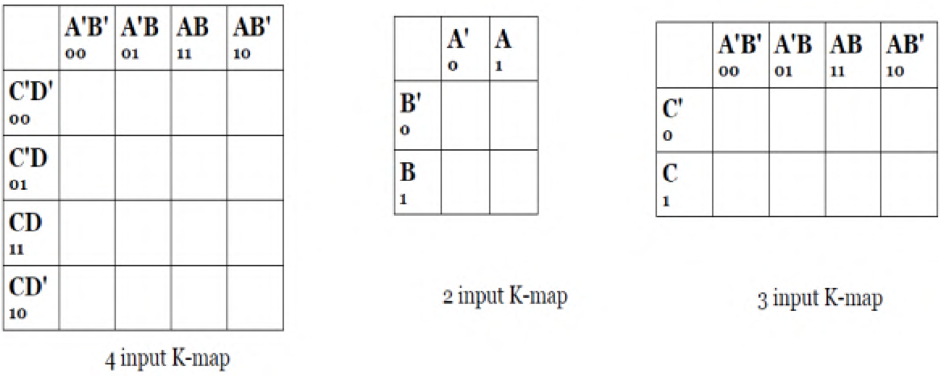


Figure 5.2: K-Map Grid

5.2.1 Overview of 3 variables K-Map

Three Variables Karnaugh's Map often known as 3 variables K-Map is a special method used in the context of digital electronics to minimize the AND, OR & NOT gates logical expressions. The variables A, B & C are used to address the cells of KMAP table to place the 1s based on the Boolean expression. A is the most significant bit (MSB) and B is the least significant bit (LSB) in the logical expressions used in the KMAP solver. Each variable A, B & C equals to value 1. Similarly, each inverted variable A, B & C equals to 0.

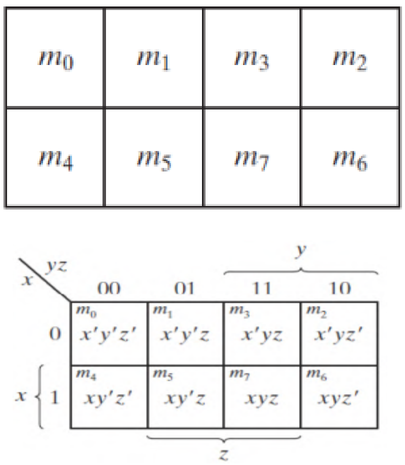


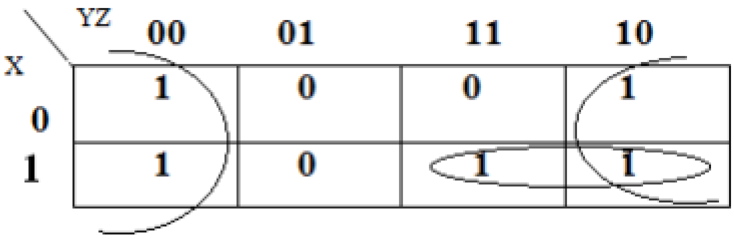
Figure 5.3: Three variables K-Map

Now we get the following truth table and we want to simplify it.

Table 5.1: Truth Table

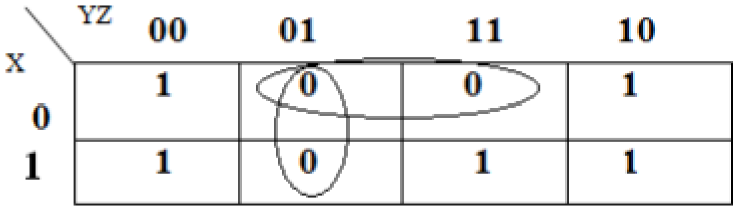
Sr. No	X	Y	Z	Output
1	0	0	0	1
2	0	0	1	0
3	0	1	0	1
4	0	1	1	0
5	1	0	0	1
6	1	0	1	0
7	1	1	0	1
8	1	1	1	1

a) Find SOP (Sum Of Product)
Solution:
By circling the ones:



F = Z' + XY

b) Find POS (Product Of Sum)
Solution:
By circling the zeros:



F' = X'Z+ Y'Z
F = (X'Z+ Y'Z)'
F = (X+Z')(Y+Z')

5.2.2 Overview of 4 variables K-Map

Four Variables Karnaugh's Map often known as 4 variables K-Map. It's an alternate method to solve or minimize the Boolean expressions based on AND, OR & NOT gates logical expressions or truth tables. The four variables A, B, C & D are the binary numbers which are used to address the min-term SOP of the Boolean expressions. The gray code conversion method is used to address the cells of K-Map table.

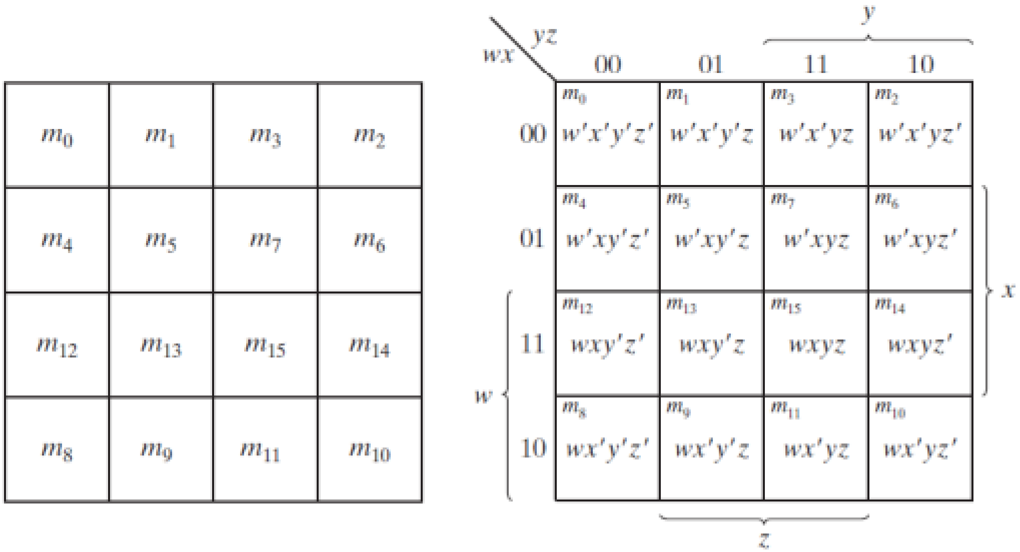
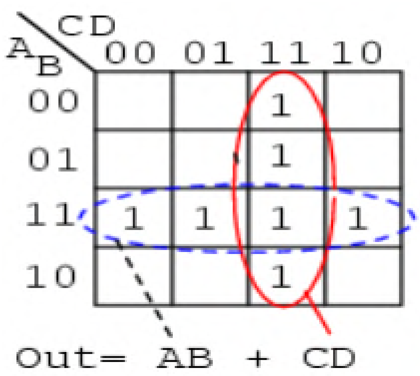


Figure 5.4: Four variables K-Map

Simplify the following Boolean function.
F = A’B’CD+A'BCD +ABCD+AB'CD+ABC'D'+ABC'D+ABCD'



5.3.2 Don’t Care Condition

One of the very significant and useful concept in simplifying the output expression using K-Map is the concept of “Don’t Cares”. The “Don’t Care” conditions allow us to replace the empty cell of a [K-Map](K-Map) to form a grouping of the variables which is larger than that of forming groups without don’t cares. While forming groups of cells, we can consider a “Don’t Care” cell as 1 or 0 or we can also ignore that cell. Therefore, “Don’t Care” condition can help us to form a larger group of cells.

A Don’t Care cell can be represented by a cross(X) in K-Maps representing a invalid combination. For example, in Excess-3 code system, the states 0000, 0001, 0010, 1101, 1110 and 1111 are invalid or unspecified. These states are called don’t cares.

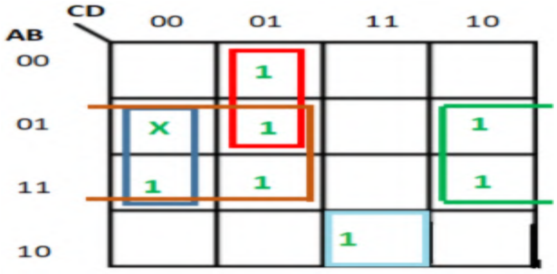
A standard SOP function having don’t cares can be converted into a POS expression by keeping don’t cares as they are, and writing the missing minterms of the SOP form as the maxterm of POS form. Similarly, a POS function having don’t cares can be converted to SOP form keeping the don’t cares as they are and writing the missing maxterms of the POS expression as the minterms of SOP expression.

For Example:

Minimise the following function in SOP minimal form using K-Maps:

i) F = m (1, 5, 6, 11, 12, 13, 14) + d (4)

The SOP K-map for the given expression is:



Therefore, SOP minimal is:

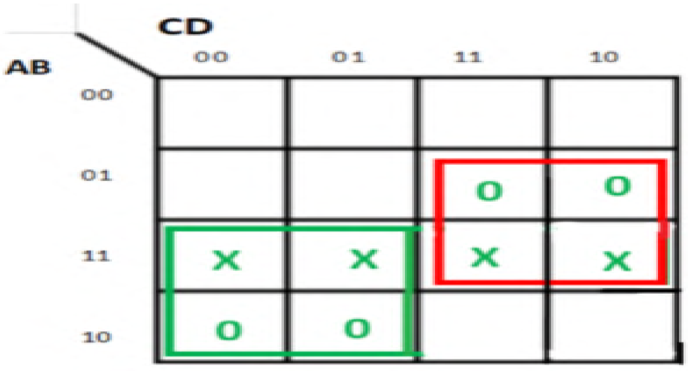
F = BC' + BCD' + A'C'D + AB'CD

ii) F (A, B, C, D) = m (0, 1, 2, 3, 4, 5) + d (10, 11, 12, 13, 14, 15)

Writing the given expression in POS form:

F (A, B, C, D) = m (6, 7, 8, 9) + d (12, 13, 14, 15)

The POS K-map for the given expression is:



Therefore, POS minimal is,

F = (A'+ C) (B' + C')

iii) F (A, B, C, D) = m (1, 2, 6, 7, 8, 13, 14, 15) + d (0, 3, 5, 12)

The SOP K-map for the given expression is:

Therefore,

F = AC'D' + A'D + A'C + AB

5.3.2.1 Significance of Don’t Care Conditions

Don’t Care conditions have the following significance in designing of the digital circuits:

1. **Simplification of the output:**
   These conditions denote inputs that are invalid for a given digital circuit. Thus, they can used to further simplify the Boolean output expression of a digital circuit.

2. **Reduction in number of gates required:**
   Simplification of the expression reduces the number of gates to be used for implementing the given expression. Therefore, don’t cares make the digital circuit design more economical.

3. **Reduced Power Consumption:**
   While grouping the terms long with don’t cares reduces switching of the states. This decreases the memory space that is required to represent a given digital circuit which in turn results in less power consumption.

4. **Represent Invalid States in Code Converters:**
   These are used in code converters. For example- In design of 4-bit BCD-to-XS-3 code converter, the input combinations 1010, 1011, 1100, 1101, 1110, and 1111 are don’t cares.

5. **Prevention of Hazards in Digital Circuits:**
   Don’t cares also prevent hazards in digital systems.

5.4 Lab Activities

5.4.2 Task-1: Simplify given logic expression using 3 variable K-Map:

Implement the resulting logic circuit and perform truth table based verification.

F (A, B, C) = Σ (1, 2, 3, 5, 6, 7)

5.4.3 Task-2: Simplify given logic expression using don't care condition and 4 variable K-Map:

Implement the resulting logic circuit and perform truth table based verification.

F (A, B, C) = Σ m (1, 5, 6, 12, 13, 14) + d (2, 4)

5.4.4 Task-3: Design a 4-bit even parity generator:

Simplify the circuit using K-Map and Implement the resulting logic circuit. Perform truth table based verification.

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: ________________ **Date: ________________**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge of Combinational Circuits Implementation using K-Maps	Makes few critical errors in applying procedural knowledge of Combinational Circuits Implementation using K-Maps	Makes some non-critical errors in applying procedural knowledge of Combinational Circuits Implementation using K-Maps	Applies the procedural knowledge of Combinational Circuits Implementation using K-Maps in perfect ways	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: ________________ **Date: ________________**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: ________________ **Date: ________________**