Experiment No 10

Design and Implementation of Counters and Shift Register

10.1 Objectives:

After completing this experiment, student will be able to:

- Describe construction and operational principle of counter.
- Design and analyze functionality of counters using state table.
- Describe construction and operational principle of Register.
- Design and analyze functionality of registers using state table.

10.2 Background Theory

A clocked sequential circuit consists of n group of flip-flops and combinational gates connected to form a feedback path. The flip-flops are essential because. In their absence, the circuit reduces to a purely combinational circuit (provided that there is no feedback among the gates). A circuit with flip-flops is considered a sequential circuit even in the absence of combinational gates. Circuits that include flip-flops are usually classified by the function they perform rather than by the name of the sequential circuit. Two such circuits are registers and counters

10.1.1 Counter

A counter is an example of a register. Its primary function is to produce a specified output pattern sequence. This sequence might correspond to the number of occurrences of an event or it might be used to control various parts of a digital system. The counting sequence is often depicted by a graph called a state diagram. A modulus-m counter (i.e., a counter with m states) has the following state diagram

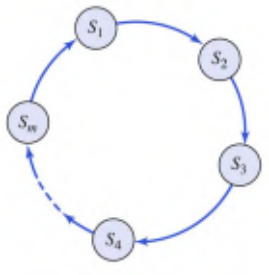


Figure: 10.1 state diagram of modulus m-counter

Each node Si denotes the states of the counter and the arrows in the graph denote the order in which the states occur. Counters are separated into two types based on how the flip-flops are triggered

- **Synchronous counter**

  Synchronous counter is the one in which all the flip flops are clocked simultaneously with the similar clock input. On the contrary, an asynchronous counter is a device in which all the flip flops that constitute that counter are clocked with different input signals at different instants of time.

- **Asynchronous counter**

  The synchronous counter, also known as parallel counter is the one in which each constituting flip flops are clocked with the same clock input simultaneously. Basically, in the synchronous counter, all the flip flops in the cascade connection are individually connected to an external clock. This facilitates the clocking of all the flip-flops constituting the counter at the same time instant with the same clock input. This means the output of each flip flop varies in synchronization with the clock input.

10.1.1.1 Binary Counter

Counter that follows the binary number sequence is called a binary counter. An N-bit binary counter consists of N flip-flops that can count in binary from 0 to $2^N - 1$. There are two types of binary counters.

- **Binary up Counter**: Counters in upward direction starting from 0 towards $2^N - 1$.
- **Binary Down Counter**: Counters in downward direction starting from $2^N - 1$ towards 0

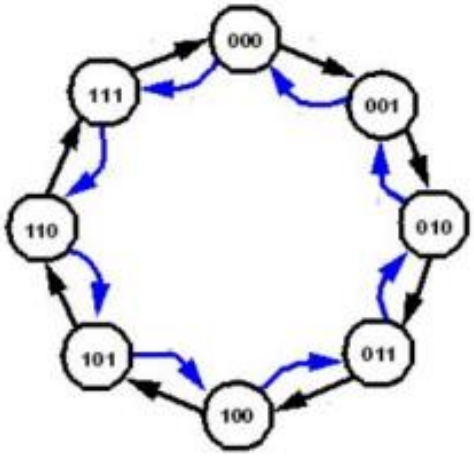
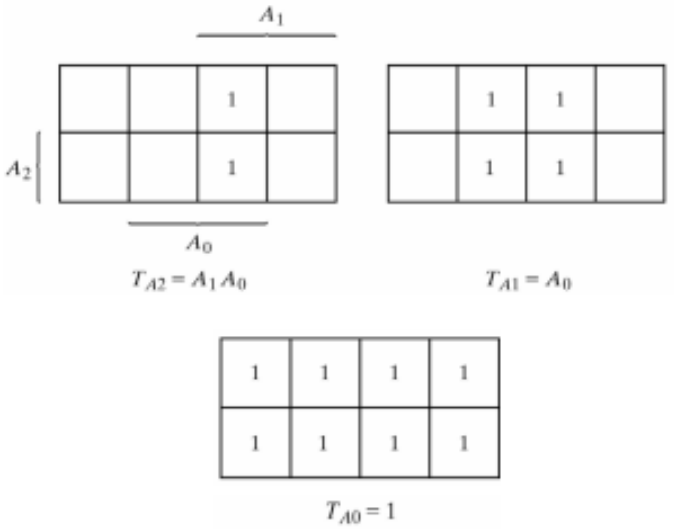


Table 3 3-bit binary counter table

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

The flip-flop input equations are specified by the Kmaps:



The input equations listed under the K-maps specify the combinational part of the counter. Including these functions with the three T flip-flops, the logic diagram of the counter is:

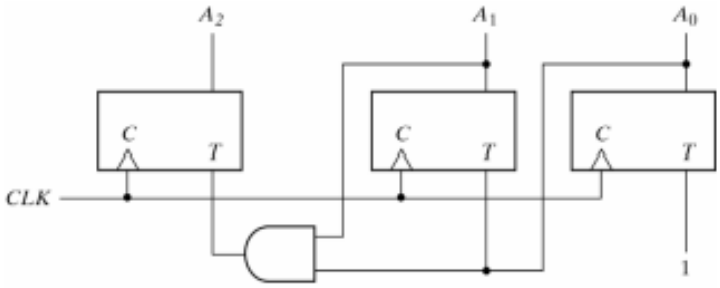


Figure 10.2 Binary Counter implementation using J-K flip-flop

Up and downward counter can be design using T flip-flop.

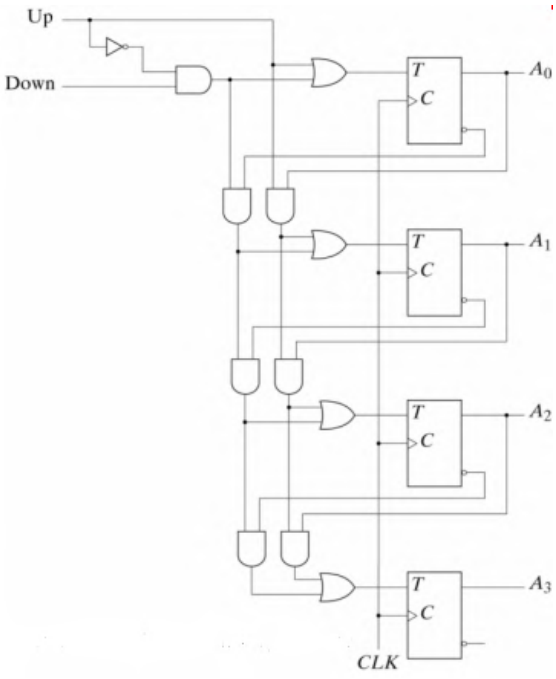


Figure 10.3 4-bit up-down binary counter using T flip-flop

Up = 1; the circuit counts up. Down = 1, Up = 0; the circuit counts down. Up = 0, Down = 0; the circuit doesn't change state. Up = 1, Down = 1, the circuit counts up.

10.1.1.2 Ripple Counter

In a ripple counter, the flip-flop output transition serves as a source for triggering other flip-flops. A 4-bit binary ripple counter (mod-16) is as follows:

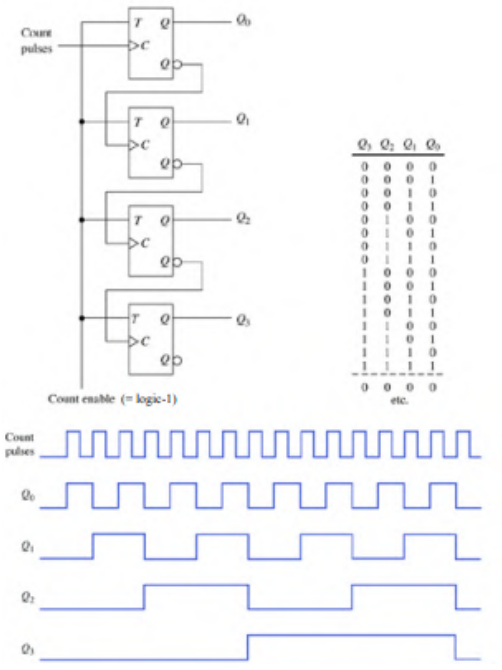


Figure 10.4 Four bit Ripple Counter

A multiple decade counter can be constructed by connecting BCD counters in cascade. A three decade counter is shown below: The inputs to the second and third decades come from Q8 of the previous decade. When Q8 in one decade goes from 1 to 0, it triggers the count for the next higher-order decade while its own goes from 9 to 0. The rippling behavior affects the overall settling time. The worst-case delay occurs when the counter goes from its 11….1-state to its 00…0-state. For an n-stage binary ripple counter, the worst-case setting time is n x tpd, where tpd is the propagation delay associated with each flip-flop.

10.1.1.3 Ring Counter

It is a circular shift register with only one flip-flop being set at any particular time, all others are cleared. The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals. A 4-bit shift register connected as a ring counter is shown below:

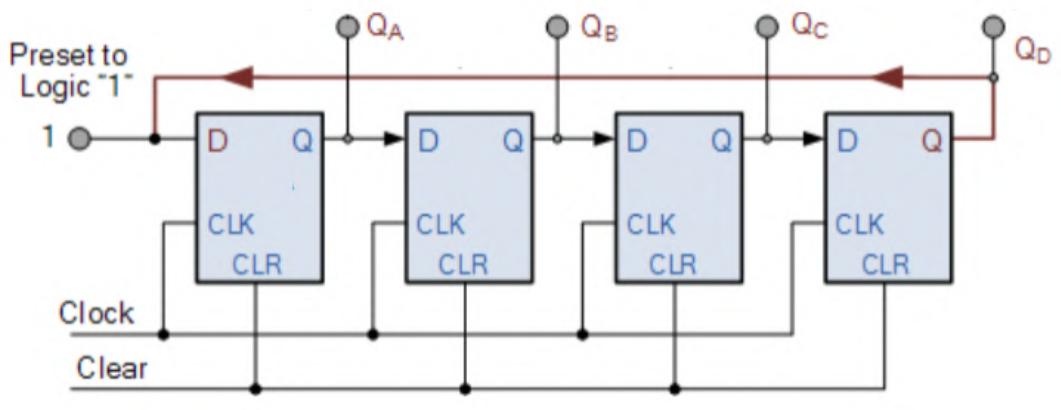


Figure 190.5 Ripple counter block diagram

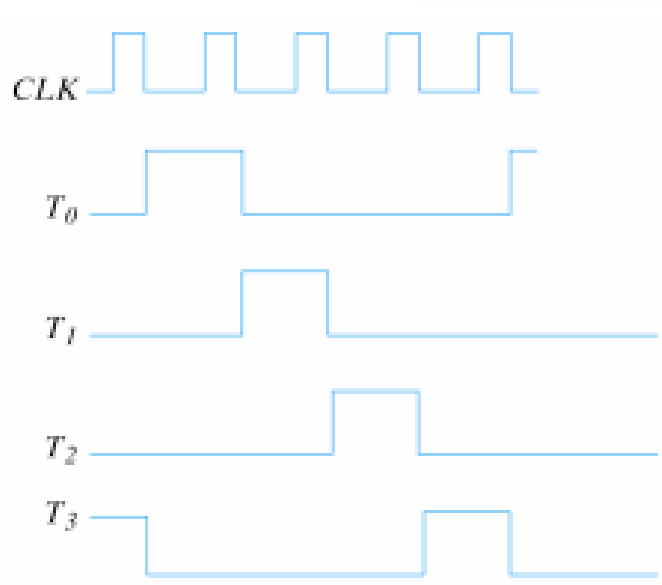


Figure 10.6 Sequence of four timing signal

10.1.1.4 Johnson Counter

An interesting variation of the ring counter is obtained if, instead of the Q output we take the Q′ of the last stage and feed it back to the first stage. A four-stage switch-tail counter is shown below:

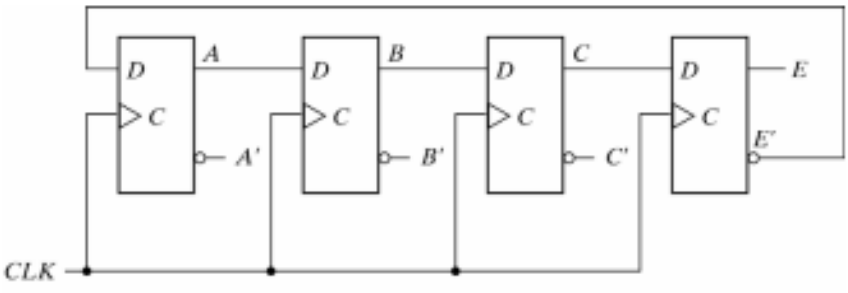


Figure 10.7 Johnson Counter Block diagram

Starting from a cleared state, the switch-tail counter goes through a sequence of eight states as listed below:

Table 4

Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

A Johnson counter is a k-bit switch-tail counter with 2k decoding gates to provide outputs for 2k timing signals.

10.1.2 Register

Register is a group of flip-flops. Its basic function is to hold information within a digital system so as to make it available to the logic units during the computing process. However, a register may also have additional capabilities associated with it. There are mainly three types of register.

- Register with parallel load
- Shift Register
- Universal Shift Register

10.1.2.1 Register with Parallel Load

Register with parallel load provides control over the information to be stored in the register through a Load control signal • When the Load signal is 1, data at the external inputs is transferred into the register • When the Load signal is 0, outputs of the flip-flops are connected to their respective inputs. Approaches to register with parallel load are:

- Controlling the clock input signal with an enabling gate: uneven propagation delays between the master clock and the inputs of flip-flops
- Controlling the D inputs: ensure that all clock pulses arrive at the same time anywhere in the system

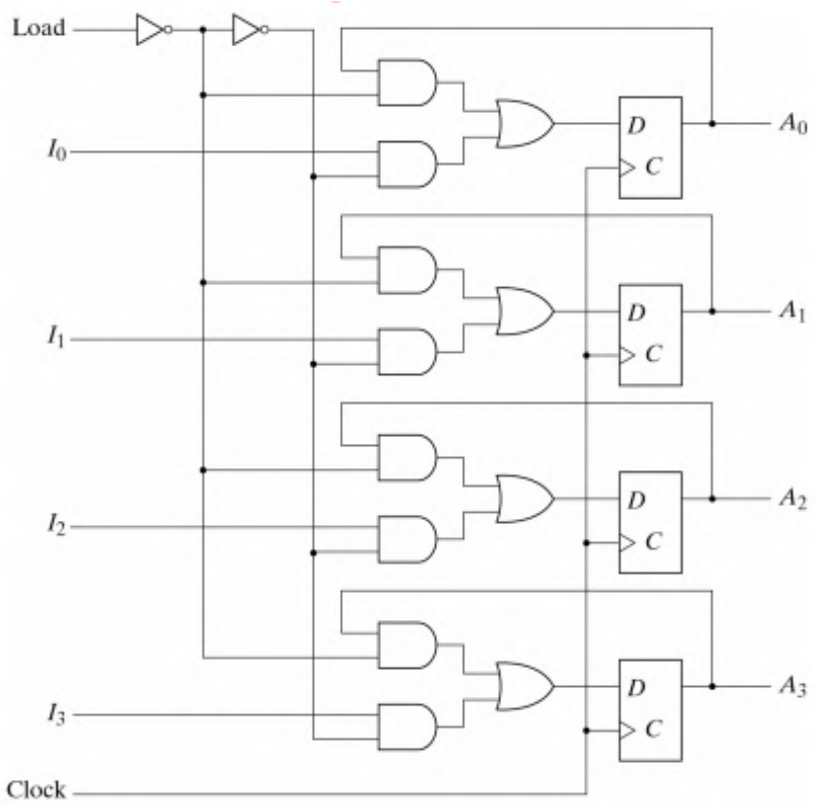


Figure 10.7 4-bit register with parallel load

The feedback connection is necessary because the D flip-flop does not have a "no change" condition. The clock pulses are applied to the C inputs at all times.

10.1.2.2 Shift Register

A register capable of shifting the binary information held in each Flip Flop to its neighboring Flip Flops, in a selected direction, is called a shift register • Information can be shifted in the left or right direction every clock cycle • N-bit Unidirectional shift right register is composed of N Flip Flops connected in cascade

Each Clock Cycle, data shifts towards right. • Data is serially fed into MSB and gets out of LSB (Serial In, Serial Out)

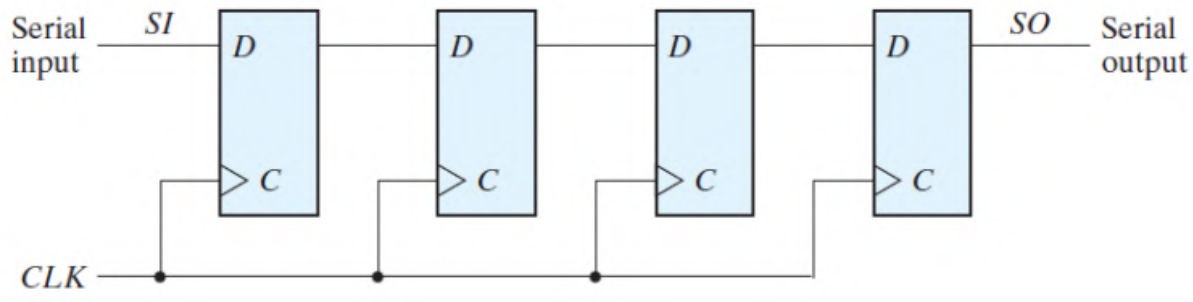


Figure 10.8 Shift Register Block Diagram

10.1.2.3 Universal Shift Register

A second general classification of shift registers consists of bidirectional shift registers. These type of registers are capable of shifting their contents either left or right depending upon the signals present on appropriate control input lines. Universal Shift Register is a general shift register that has the following capabilities:

- Left shift
- Right shift
- Parallel Load
- Data Unchanged

Table 3 Mode Control of Universal Shift Register

Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

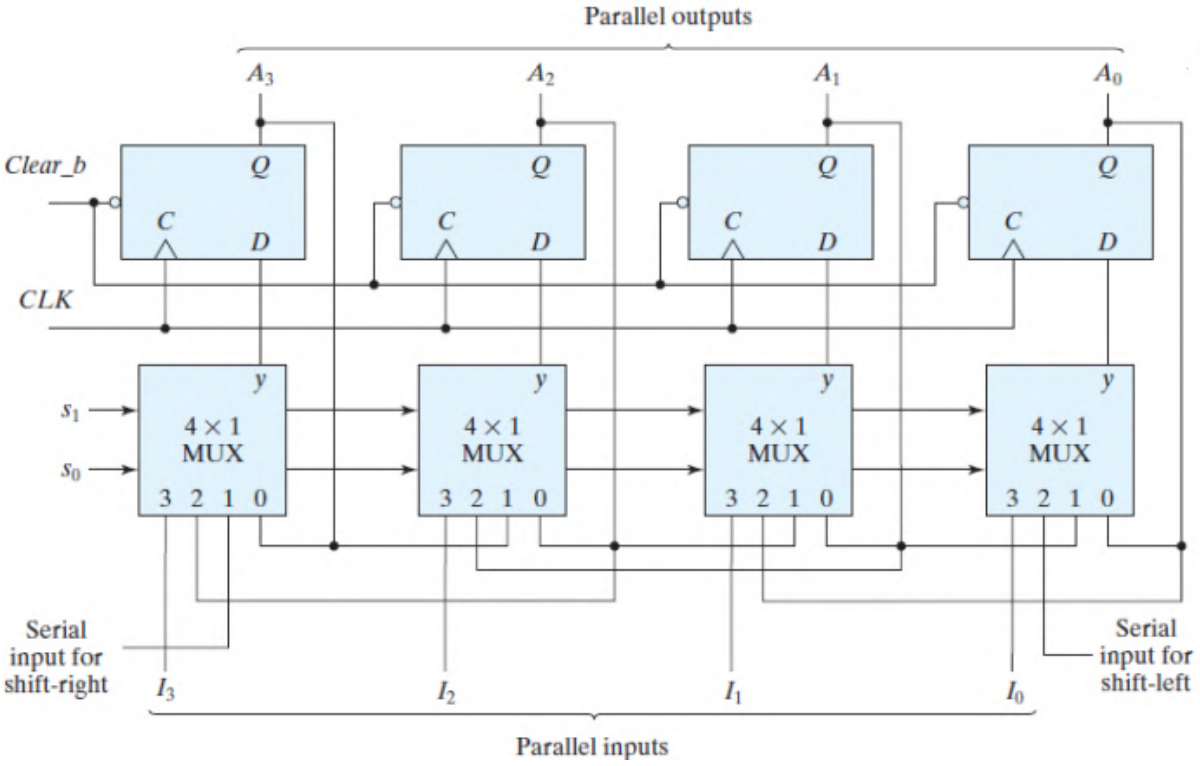


Figure 10.9 Universal Shift Register Block Diagram

10.2 Lab Activities

10.2.1 Task-1:

Design and Implement a 3-bit binary counter using T Flip-Flop.

10.2.2 Task-2:

Implement a 4-bit Johnson Counter and verify its functionality using state table.

10.2.3 Task-3:

Implement a 4-bit Universal Shift Register and verify its functionality using state table.

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Psychomotor)

Total Marks: 100

Criteria (Max Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S< 70%	Level 3 70% ≤ S< 90%	Level 4 90%≤ S ≤100%	Score (S)
Procedural Awareness (20)	Selects inappropriate skills and/or strategies required by the task	Selects and applies appropriate skills and/or strategies required by the task with some errors	Selects and applies the appropriate strategies and/or skills specific to the task without significant errors	Selects and applies appropriate strategies and/or skills specific to the task without any error	
Practical Implementation (30)	Makes several critical errors in applying procedural knowledge of counters and shift register	Makes few critical errors in applying procedural knowledge of counters and shift register	Makes some non-critical errors in applying procedural knowledge of counters and shift register	Applies the procedural knowledge of counters and shift register in perfect ways	
Safety (10)	Requires constant reminders to follow safety procedures	Requires some reminders to follow safety procedures	Follows safety procedures with only minimal reminders	Routinely follows safety procedures	
Use of Tool/Equipment (20)	Uses tools, equipment and materials with limited competence	Uses tools, equipment and materials with some competence	Uses tools, equipment and materials with considerable competence	Uses tools, equipment and materials with a high degree of competence	
Participation to Achieve Group Goals (10)	Shows little commitment to group goals and fails to perform assigned roles	Demonstrates commitment to group goals, but has difficulty performing assigned roles	Demonstrates commitment to group goals and carries out assigned roles effectively	Actively helps to identify group goals and works effectively to meet them in all roles assumed	
Interpersonal Skills in Group Work (10)	Rarely interacts positively within a group, even with prompting	Interacts with other group members if prompted	Interacts with all group members spontaneously	Interacts positively with all group members and encourages such interaction in others	
				Marks Obtained	

Instructor's Signature: _____ **Date: _____**

LABORATORY SKILLS ASSESMENT (Affective)

Total Marks: 40

Criteria (Max. Marks)	Level 1 0% ≤ S < 50%	Level 2 50% ≤ S < 70%	Level 3 70% ≤ S < 90%	Level 4 90% ≤ S ≤ 100%	Score (S)
Introduction (5)	Very little background information provided or information is incorrect	Introduction is brief with some minor mistakes	Introduction is nearly complete, missing some minor points	Introduction complete and well-written; provides all necessary background principles for the experiment	
Procedure (5)	Many stages of the procedure are not entered on the lab report.	Many stages of the procedure are entered on the lab report.	The procedure could be more efficiently designed but most stages of the procedure are entered on the lab report.	The procedure is well designed and all stages of the procedure are entered on the lab report.	
Data Record (10)	Data is brief and missing significant pieces of information.	Data provides some significant information and has few critical mistakes.	Data is almost complete but has some minor mistakes.	Data is complete and relevant. Tables with units are provided. Graphs are labeled. All questions are answered correctly.	
Data Analysis (10)	Data is presented in very unclear manner. Error analysis is not included.	Data is presented in ways (charts, tables, graphs) that are not clear enough. Error analysis is included.	Data is presented in ways (charts, tables, graphs) that can be understood and interpreted. Error analysis is included.	Data are presented in ways (charts, tables, graphs) that best facilitate understanding and interpretation. Error analysis is included.	
Report Quality (10)	Report contains many errors.	Report is somewhat organized with some spelling or grammatical errors.	Report is well organized and cohesive but contains some grammatical errors.	Report is well organized and cohesive and contains no grammatical errors. Presentation seems polished.	
				Marks Obtained	

LABORATORY SKILLS ASSESSMENT (Cognitive)

Total Marks: 10

(If any) **Marks Obtained**	

Instructor's Signature: _____ **Date: _____**