Experiment No 10

External Interrupts of STM32

Objectives:

- To learn the basic difference between Interrupt and Polling.
- To learn about the External Interrupts of STM32F103 and their programming using Keil.

10.1 Interrupt & Polling:

The main difference between interrupt and polling is that, in the case of an interrupt, the device notifies the CPU that it requires attention while, in the case of polling, the CPU continuously checks the status of the device to find whether it requires attention.

Generally, an operating system is the layer between the hardware and user programs. Here, the CPU is the component that handles the tasks of the entire computer system. Sometimes, it is necessary to pause the currently executing task and perform immediate actions. Two such mechanisms are interrupts and polling.

10.2 External Interrupts of STM32F103:

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 externalinterrupt lines.

Nested Vector Interrupt Controller (NVIC):

The STM32F103xx performance line embeds a nested vectored interrupt controller able tohandle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex®- M3) and 16 priority levels.

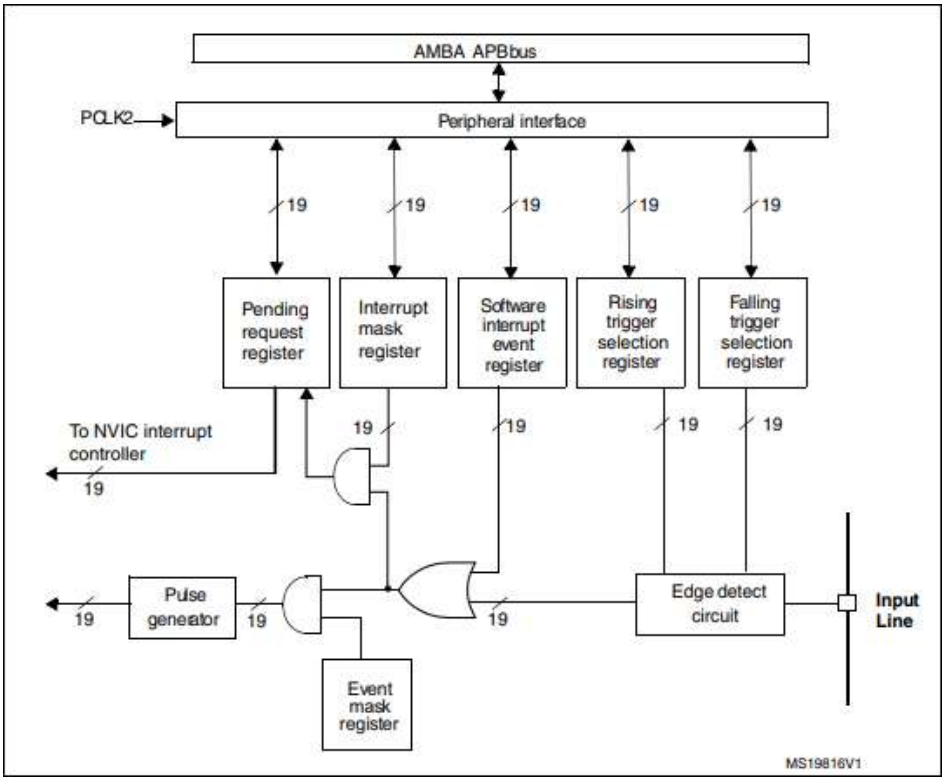
- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

10.3 Main features of External Interrupts:

The EXTI controller main features are the following:

• Independent trigger and mask on each interrupt/event line
• Dedicated status bit for each interrupt line
• Generation of up to 20 software event/interrupt requests
• Detection of external signal with pulse width lower than APB2 clock period. Refer to the electrical characteristics section of the datasheet for details on this parameter.



• Figure 1: External Interrupt/Event Controller Block Diagram

Following is the GPIO mapping of the External Interrupts.

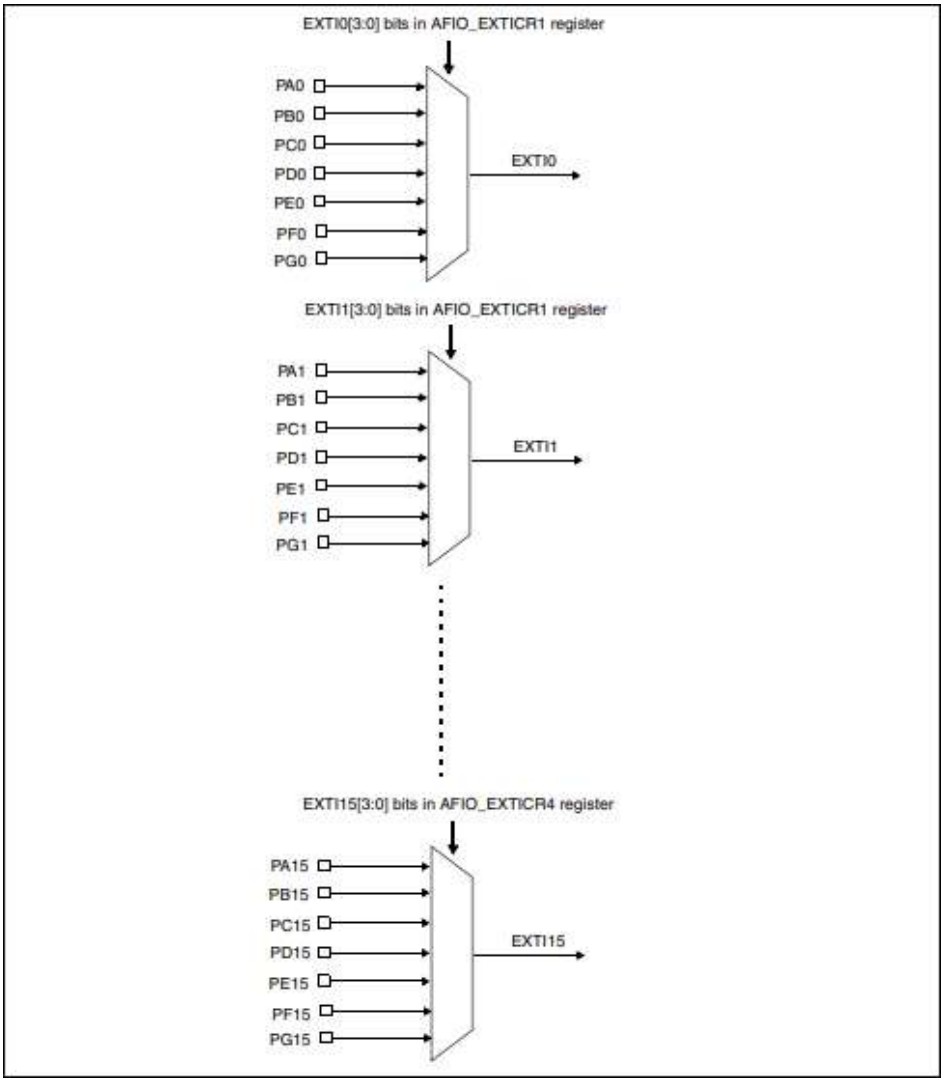


Figure 2: External Interrupt/Event GPIO Mapping

10.4 Required Configurations for External Interrupt:

```
void EXTI15_10_Init()
{
	// Initalization struct
	GPIO_InitTypeDef GPIO_InitStruct;
	EXTI_InitTypeDef EXTI_InitStruct;
	NVIC_InitTypeDef NVIC_InitStruct;

	// Initialize PB12 as input with pull-up resistor
	RCC_APB2PeriphClockCmd(RCC_APB2Periph_GPIOB, ENABLE);
	GPIO_InitStruct.GPIO_Pin = GPIO_Pin_12;
	GPIO_InitStruct.GPIO_Mode = GPIO_Mode_IPU;
	GPIO_InitStruct.GPIO_Speed = GPIO_Speed_2MHz;
	GPIO_Init(GPIOB, &GPIO_InitStruct);

	// Initialize PB12 to EXTI
	RCC_APB2PeriphClockCmd(RCC_APB2Periph_AFIO, ENABLE);
	GPIO_EXTILineConfig(GPIO_PortSourceGPIOB, GPIO_PinSource12);

	// Initialize EXTI line 12 for PB12
	EXTI_InitStruct.EXTI_Line = EXTI_Line12;
	EXTI_InitStruct.EXTI_Mode = EXTI_Mode_Interrupt;
	EXTI_InitStruct.EXTI_Trigger = EXTI_Trigger_Rising;
	EXTI_InitStruct.EXTI_LineCmd = ENABLE;
	EXTI_Init(&EXTI_InitStruct);

	// Initialize NVIC for EXTI15_10 IRQ channel
	NVIC_InitStruct.NVIC_IRQChannel = EXTI15_10_IRQn;
	NVIC_InitStruct.NVIC_IRQChannelPreemptionPriority = 0x00;
	NVIC_InitStruct.NVIC_IRQChannelSubPriority = 0x00;
	NVIC_InitStruct.NVIC_IRQChannelCmd = ENABLE;
	NVIC_Init(&NVIC_InitStruct);
}
```

10.5 Libraries to include:

Interrupt.c

```c
#include "stm32f10x.h"
#include "stm32f10x_rcc.h"
#include "stm32f10x_gpio.h"
#include "stm32f10x_exti.h"
//#include "delay.h"

void EXTI15_10_Init(void);
void GPIO_Config();
void delay(unsigned int nCount);

GPIO_InitTypeDef GPIO_InitStruct;

```

10.6 Main Function:

```c
int main(void)
{
  // Initialize exernal interrupt
  EXTI15_10_Init();

  GPIO_Config();

  while (1)
  {
    // Blink LED on PC13
    GPIO_ResetBits(GPIOC, GPIO_Pin_13);
    delay(10);
    GPIO_SetBits(GPIOC, GPIO_Pin_13);
    delay(10);
  }
}
```

10.7 Interrupt Handler:

```
30  void EXTI15_10_IRQHandler(void)
31  {
32    // Checks whether the interrupt is from EXTI12 or not
33    if (EXTI_GetITStatus(EXTI_Line12))
34    {
35      // Blink LED on PB13 5 times
36      int i;
37      for (i = 0; i < 10; i++)
38      {
39        GPIO_ResetBits(GPIOB, GPIO_Pin_13);
40        delay(10);
41        GPIO_SetBits(GPIOB, GPIO_Pin_13);
42        delay(10);
43      }
44      // Clear pending bit
45      EXTI_ClearITPendingBit(EXTI_Line12);
46    }
47  }
```

10.8 GPIO Configuration & Delay Function:

```
82  void GPIO_Config()
83  {
84    // Initialize PB13 as push-pull output for LED
85    RCC_APB2PeriphClockCmd(RCC_APB2Periph_GPIOB, ENABLE);
86    GPIO_InitStruct.GPIO_Pin = GPIO_Pin_13;
87    GPIO_InitStruct.GPIO_Mode = GPIO_Mode_Out_PP;
88    GPIO_InitStruct.GPIO_Speed = GPIO_Speed_2MHz;
89    GPIO_Init(GPIOB, &GPIO_InitStruct);
90
91    // Initialize PC13 as push-pull output for LED
92    RCC_APB2PeriphClockCmd(RCC_APB2Periph_GPIOC, ENABLE);
93    GPIO_InitStruct.GPIO_Pin = GPIO_Pin_13;
94    GPIO_InitStruct.GPIO_Mode = GPIO_Mode_Out_PP;
95    GPIO_InitStruct.GPIO_Speed = GPIO_Speed_2MHz;
96    GPIO_Init(GPIOC, &GPIO_InitStruct);
97  }
98  // Delay function
99  void delay(unsigned int nCount)
100 {
101   unsigned int i, j;
102     for (i = 0; i < nCount; i++)
103       for (j = 0; j < 0x2AFF; j++);
104 }
```

10.9 Programming in KEIL:

To program the External Interrupt in Keil, the first step is to create a new uVision Project and selecting the device which is STM32F103C8 just like we already did in the previous labs.

After saving the project in your desired directory, the device will be selected in the 'Select Device for Target' dialogue box.

After that, include the libraries of Core, GPIO, Startup, EXTI, Framework & RCC as shown in the figure below:

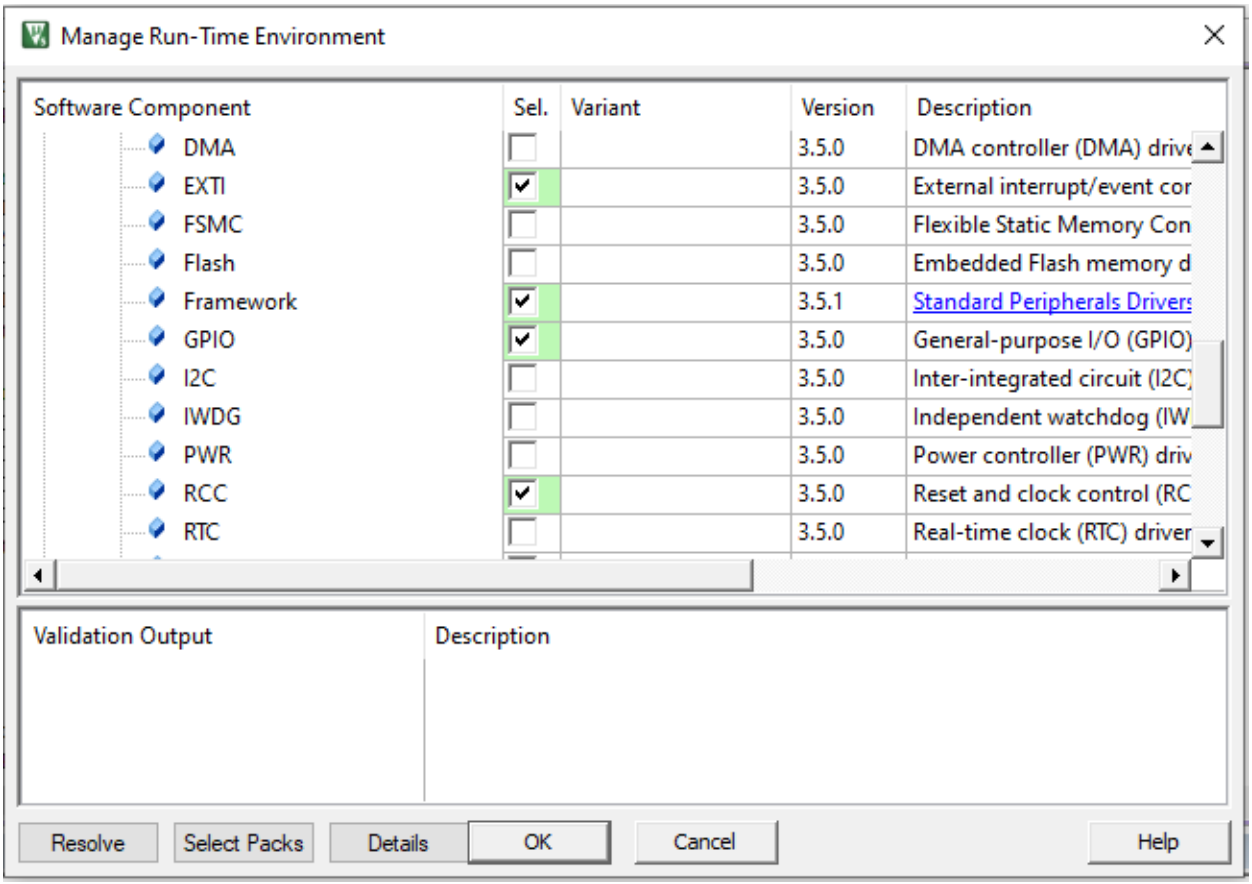


Figure 3: Libraries to Include

Lab Task to Perform

Activity 01:

Write a C-Program that invokes an interrupt service routine to service an external interrupt. External interrupt shall be executed by pressing a push button. The routine shall toggle a LED for 10 times. Before and after the interrupt, the program shall toggle another LED in the while loop of the main function.

Activity 02:

Write a C-Program that invokes multiple interrupt service routines to service 3 external interrupts. External interrupts shall be executed by pressing 3 push buttons. The routines shall display, which interrupt is invoked, on a 16x2 LCD. Before and afterthe interrupt, the program shall only display the student's name on the LCD.

Lab Task (Cognitive)

CLO1 Cognitive Questionnaire C3

Question 1:

A push button on pin PA0 must trigger an external interrupt on the falling edge. The ISR toggles an LED.

a) Differentiate between interrupt-driven and polling-based input handling and state one advantage of using interrupts. **[3 Marks]**

b) List the configuration steps required to enable the falling-edge interrupt for PA0 (pin-to-EXTI mapping, trigger selection, masking and NVIC). **[3 Marks]**

c) State what the ISR must do before returning and what happens if this is not done. **[2 Marks]**

d) Can PA0 and PB0 be used as external interrupt sources at the same time? Justify your answer. **[2 Marks]**

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ Date: _____

LABORATORY SKILLS ASSESSMENT (Cognitive)

Obtained Marks	**/10**

Instructor's Signature: _____ Date: _____

LABORATORY SKILLS ASSESSMENT (Psychomotor)

Psychomotor Activity 1: Experimental Setup

S. No	Criteria	Performance	Description	Marks
1	**Interrupt Hardware & Software Setup (4)**	Level 4	Correctly prepares the required interrupt hardware and software setup for the experiment independently and according to the laboratory requirements.	4
		Level 3	Correctly prepares the required interrupt hardware and software setup with minor errors or assistance.	3
		Level 2	Partially prepares the required interrupt hardware and software setup and requires considerable assistance.	2
		Level 1	Shows limited ability to prepare the required interrupt hardware and software setup and requires substantial assistance.	1
2	**EXTI & NVIC Configuration (4)**	Level 4	Correctly prepares the required EXTI and NVIC configuration for the experiment independently and according to the laboratory requirements.	4
		Level 3	Correctly prepares the required EXTI and NVIC configuration with minor errors or assistance.	3
		Level 2	Partially prepares the required EXTI and NVIC configuration and requires considerable assistance.	2
		Level 1	Shows limited ability to prepare the required EXTI and NVIC configuration and requires substantial assistance.	1
3	**Trigger & Priority Parameters (2)**	Level 2	Correctly sets the required trigger and priority parameters for the experiment.	2
		Level 1	Sets the basic trigger and priority parameters with minor errors or assistance.	1
Total Obtained				**/10**

If a student is absent:

Criteria	Description	Marks
Absent	Student is absent from the laboratory activity.	**0**

Psychomotor Activity 2: Implementation + Results

S. No	Criteria	Performance	Description	Marks
1	**ISR & Main Program Implementation (4)**	Level 4	Correctly implements the assigned ISR and main program independently while following appropriate laboratory practices.	4
		Level 3	Implements the assigned ISR and main program with minor errors or assistance and generally follows proper laboratory practices.	3
		Level 2	Partially implements the assigned ISR and main program and requires considerable assistance or repeated guidance.	2
		Level 1	Implementation of the assigned ISR and main program is largely incomplete, requires substantial assistance, or shows poor adherence to proper laboratory and safety practices.	1
2	**Execution & Debugging (2)**	Level 2	Correctly performs the required execution and debugging and verifies the expected operation.	2
		Level 1	Performs the basic execution and debugging with minor errors or assistance.	1
3	**Interrupt Response & Output Analysis (4)**	Level 4	Obtains correct interrupt response and output analysis and appropriately verifies and interprets the required experimental results.	4
		Level 3	Obtains mostly correct interrupt response and output analysis with minor errors in verification or interpretation.	3
		Level 2	Obtains partially correct interrupt response and output analysis with noticeable errors or omissions.	2
		Level 1	Interrupt response and output analysis is largely incorrect or incomplete and requires substantial assistance.	1
Total Obtained				**/10**

If a student is absent:

Criteria	Description	Marks
Absent	Student is absent from the laboratory activity.	**0**

Instructor's Signature: _____ Date: _____

LABORATORY SKILLS ASSESSMENT (Affective)

Affective Activity: Lab Report + Viva Voce

S. No	Criteria	Performance	Description	Marks
1	**Lab Report Completeness & Organization (4)**	Level 4	Report is complete, well-organized, properly presented, and demonstrates responsible completion of the assigned laboratory work.	4
		Level 3	Report is complete with minor omissions or organizational issues and demonstrates satisfactory responsibility for the assigned work.	3
		Level 2	Report is partially complete with several omissions and demonstrates limited responsibility for the assigned work.	2
		Level 1	Report has major omissions or poor organization and demonstrates minimal responsibility for the assigned work.	1
2	**Interrupt Output & Conclusion (2)**	Level 2	The interrupt output and conclusion are correctly presented and discussed, demonstrating ownership of the assigned work.	2
		Level 1	The interrupt output and conclusion are presented with minor errors or omissions.	1
3	**Viva Voce (4)**	Level 4	Clearly explains the assigned experiment, interrupt handling, EXTI/NVIC configuration, program explanation, working, and results, demonstrating individual responsibility, participation, and effective communication.	4
		Level 3	Explains most of the assigned experiment and results correctly, with minor difficulty, and demonstrates good individual participation.	3
		Level 2	Explains basic aspects of the assigned experiment with some prompting and demonstrates basic participation.	2
		Level 1	Demonstrates limited understanding or involvement and requires substantial prompting to explain the assigned work.	1
Total Obtained				**/10**

The student has not submitted the report and has not appeared in the Viva Voce.

Criteria	Description	Marks
Lab Report and Results Not Submitted	Student has not submitted the report and results file.	**0**
Absent in Viva Voce	Student is absent from the viva voce.	**0**

Instructor's Signature: _____ Date: _____