Experiment No 3

Implementation of RAM and ROM memory blocks in LogiSim

3.1 Objectives

After completing this experiment, student will be able to:

- Understand RAM and ROM basic operations.
- Implement RAM and ROM memory blocks in LogiSim.
- Store and Load data in RAM and ROM.
- Experience Counter, Bit Extender, TTY and Random Generator components of LogiSim.

3.2 Background Theory

RAM (Random Access Memory) is a type of volatile memory in a computer system that serves as a temporary workspace for actively running programs and data. It provides fast access to data for the CPU (Central Processing Unit), allowing it to quickly read and write information during program execution. RAM's volatile nature means that its contents are lost when the computer is powered off, necessitating regular saving of data to non-volatile storage like hard drives or SSDs. This temporary storage capability enables multitasking, as RAM can hold multiple programs and data simultaneously, facilitating smooth operation without constantly accessing slower storage mediums.

On the other hand, ROM (Read-Only Memory) is a type of non-volatile memory that stores essential software and firmware instructions required for booting up the computer and initializing hardware components. Unlike RAM, ROM's contents are permanent and cannot be easily modified or erased during normal operation. It holds critical instructions that are crucial for the system's basic functionality, such as the BIOS (Basic Input/Output System) or firmware for various hardware components. ROM plays a foundational role in the startup process, ensuring that the computer can begin executing instructions even before other forms of storage, like hard drives, become accessible.

3.2.1 RAM in LogiSim

In Logisim, RAM (Random Access Memory) refers to a component that can store binary data in a manner that allows for both reading and writing. You can use RAM in LogiSim as shown in Figure: 3.1.

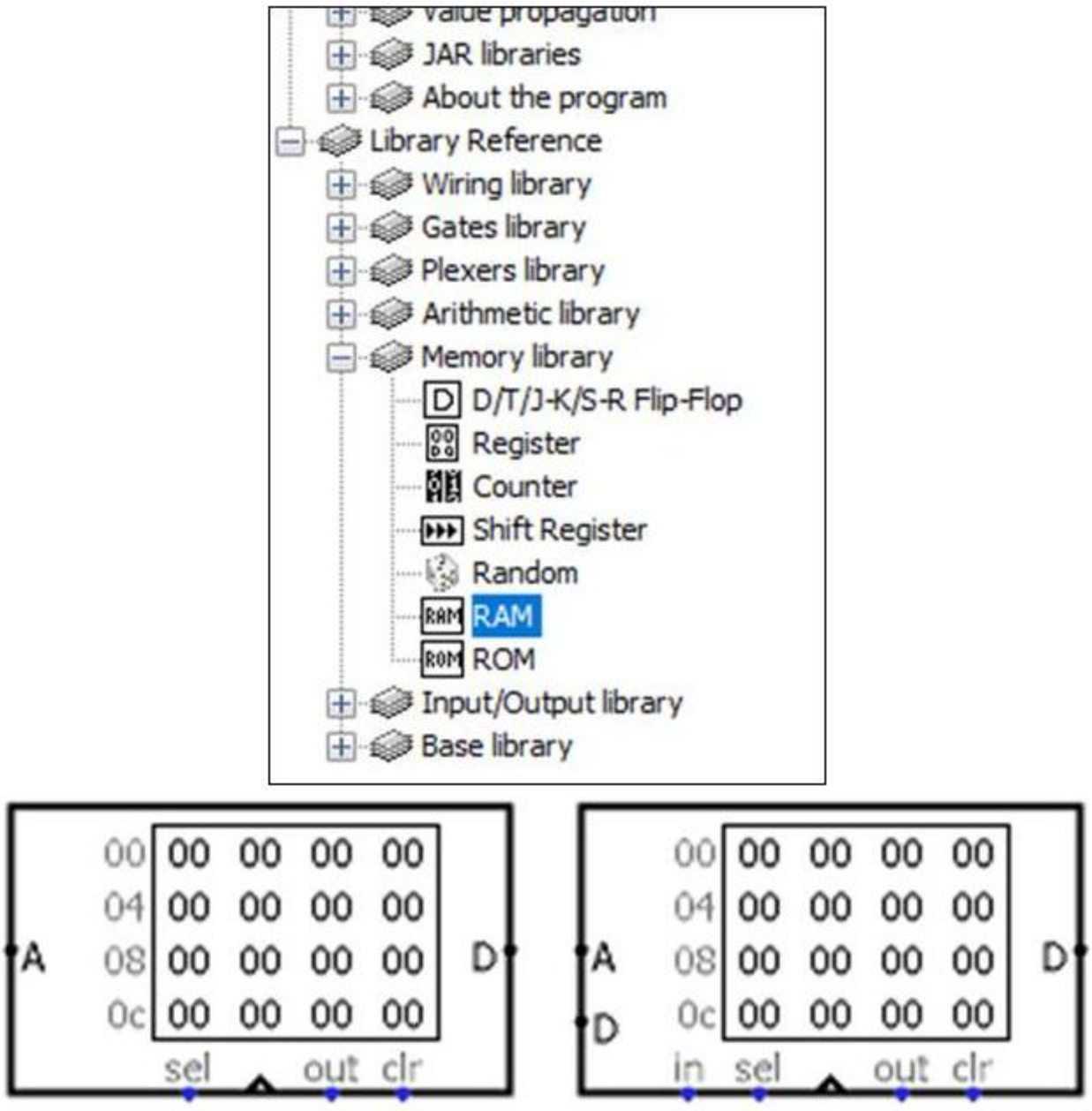


Figure 3.1: Appearance of RAM in LogiSim

The RAM component, easily the most complex component in Logisim's built-in libraries, stores up to 2^{24} = 16,777,216 values (specified in the Address Bit Width attribute), each of which can

include up to to 32 bits (specified in the Data Bit Width attribute). The circuit can load and store values in RAM. Also, the user can modify individual values interactively via the Poke Tool, or the user can modify the entire contents via the Menu Tool.

Current values are displayed in the component. Addresses displayed are listed in gray to the left of the display area. Inside, each value is listed using hexadecimal. The value at the currently selected address will be displayed in inverse text (white on black).

The RAM component supports three different interfaces, depending on the Data Interface attribute.

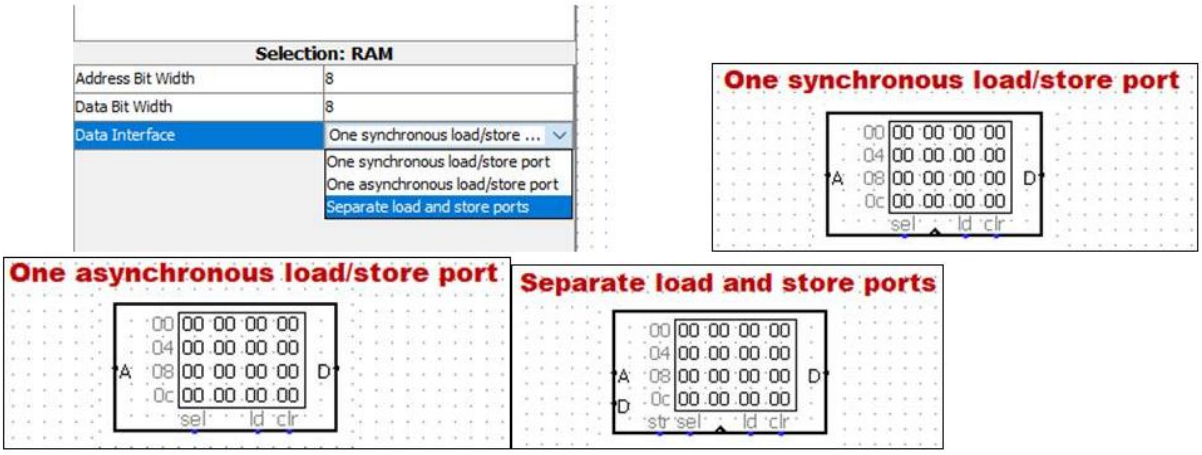


Figure 3.2: Different Interfaces of RAM in LogiSim

3.2.1.1 One synchronous load/store port (default)

The component includes a single port on its east side that serves for both loading and storing data. Which it performs depends on the input labeled *ld*: 1 (or floating) indicates to load the data at the address designated on the component's west side, and 0 indicates to store the data given on the

port. To transmit data into and out of the component, you will need to use a Controlled Buffer component, as illustrated below.

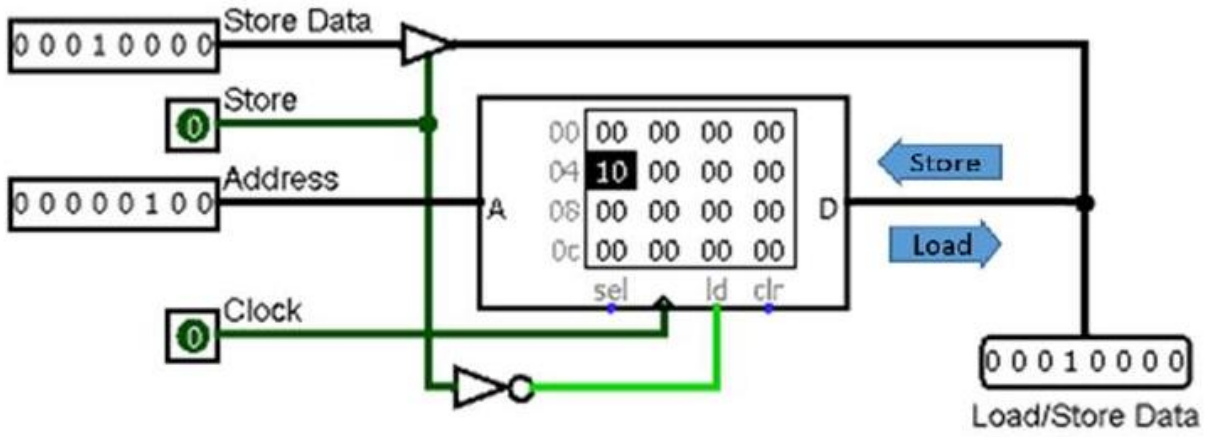


Figure 3.3: One synchronous load/store port (default) of RAM in LogiSim

3.2.1.2 One asynchronous load/store port

This is the same as above, except that there is no clock. The value found on the data bus is stored into memory whenever the *ld* input is 0. If, while the *ld* input is 0, the address or data changes, then an additional store occurs. This option is meant to more closely approximate the interface of many available random-access memories.

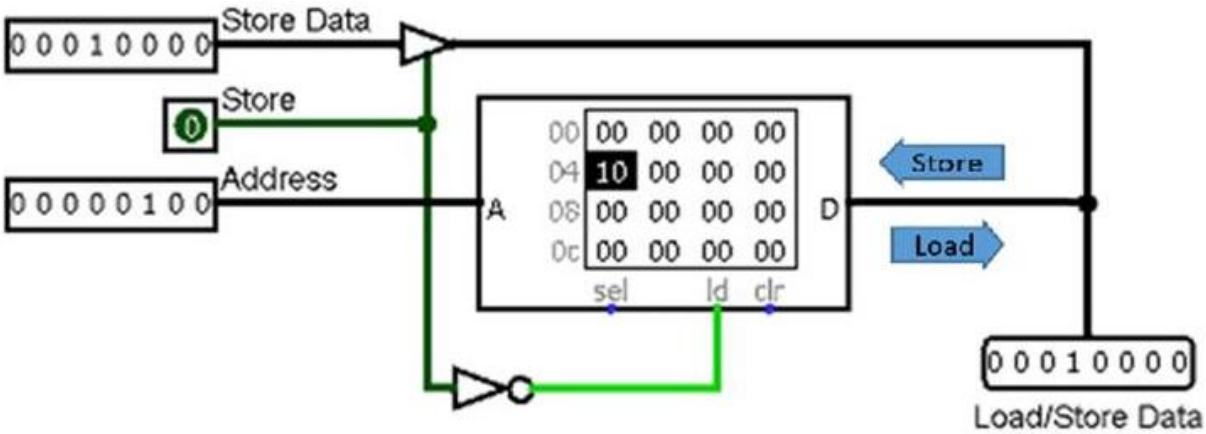


Figure 3.4: One synchronous load/store port of RAM in LogiSim

3.2.1.3 Separate load and store ports

Two data ports are provided - one on the west side for storing data, and another on the east side for loading data. This option removes the necessity of dealing with the Controlled Buffer and so it is easier to use.

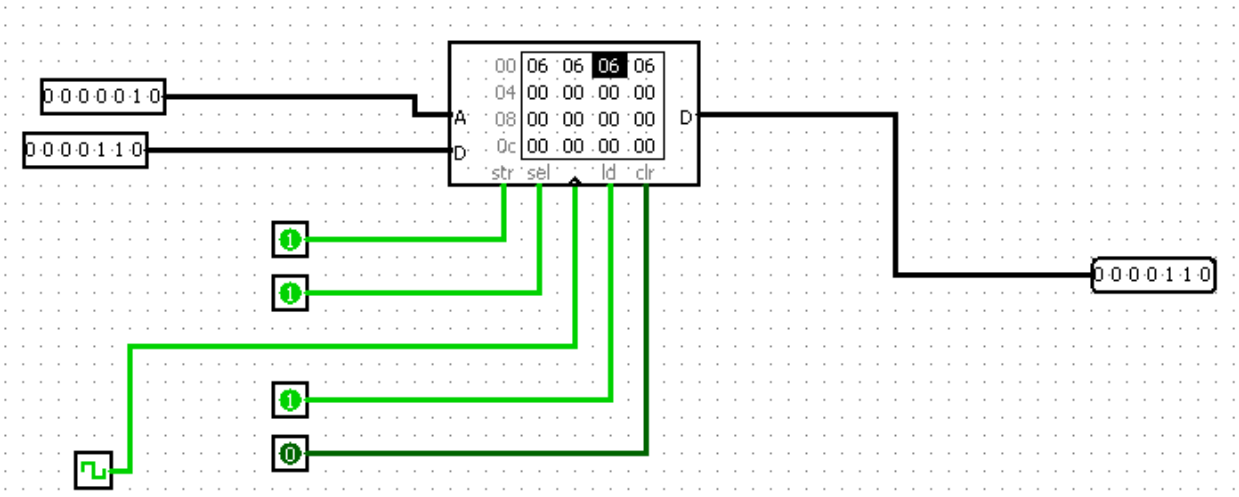


Figure 3.5: Separate load/store port of RAM in LogiSim

3.2.1.4 Pins

A on west edge (input, bit width matches Address Bit Width attribute)
Selects which of the values in memory is currently being accessed by the circuit.

D on west edge (input, bit width matches Data Bit Width attribute)
This input is present only if "separate load and store ports" is selected for the Data Interface attribute. When a store is requested (via the clock changing from 0 to 1 while *sel* and *str* are both 1 or floating), the value found at this port is stored into memory at the currently selected address.

D on east edge (input/output or output, bit width matches Data Bit Width attribute)
If *sel* and *ld* are 1 or floating, then the RAM component emits the value found at the currently selected address on this port. If there is a single load/store port, the value read from this port is stored whenever a store is requested.

str on south edge (input, bit width 1)
Store: This input is present only if "separate load and store ports" is selected for the Data Interface attribute. When it is 1 or floating, a clock pulse will result in storing the data found on the west edge into memory (provided the *sel* input is also 1 or floating).

sel on south edge (input, bit width 1)

Chip select: This input enables or disables the entire RAM module, based on whether the value is 1/floating or 0. The input is meant primarily for situations where you have multiple RAM units, only one of which would be enabled at any time.

Triangle on south edge (input, bit width 1)

Clock input: This is absent when the Data Interface attribute's value is "One asynchronous load/store port." In other circumstances, when *ld* is 0, and this input rises from 0 to 1 (and *sel* is 1/undefined and *clr* is 0), then the value at the currently selected address changes to whatever value is at the *D* pin. As long as the clock input remains 0 or 1, though, the *D* value will not be stored into memory.

ld on south edge (input, bit width 1)

Load: Selects whether the RAM should emit (on *D*) the value at the current address (*A*). This output behavior is enabled if *out* is 1 or undefined; if *out* is 0, then no value is pushed onto *D* - but if there is a combined load/store port, stores will be enabled.

clr on south edge (input, bit width 1)

Clear: When this is 1, all values in memory are pinned to 0, no matter what the other inputs are.

3.2.1.5 Attributes

When the component is selected or being added, the digits '0' through '9' alter its Address Bit Width attribute and Alt-0 through Alt-9 alter its Data Bit Width attribute.

Address Bit Width

The bit width of the address bits. The number of values stored in RAM is $2^{addrBitWidth}$.

Data Bit Width

The bit width of each individual value in memory.

Data Interface

Configures which of the three interfaces are used for communicating data into and out of the component.

3.2.2 ROM in LogiSim

The ROM component stores up to 16,777,216 values (specified in the Address Bit Width attribute), each of which can include up to to 32 bits (specified in the Data Bit Width attribute). A circuit can access the current values in ROM, but it cannot change them. The user can modify individual values interactively via the Poke Tool, or the user can modify the entire contents via the Menu Tool.

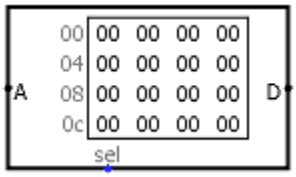


Figure 3.6: Appearance of ROM in LogiSim

Unlike the RAM component, the ROM component's current contents are stored as an attribute of the component. Thus, if a circuit containing a ROM component is used twice, then both ROM components will hold the same values. Also because of this behavior, the current ROM contents are stored in files created by Logisim.

Current values are displayed in the component. Addresses displayed are listed in gray to the left of the display area. Inside, each value is listed using hexadecimal. The value at the currently selected address will be displayed in inverse text (white on black).

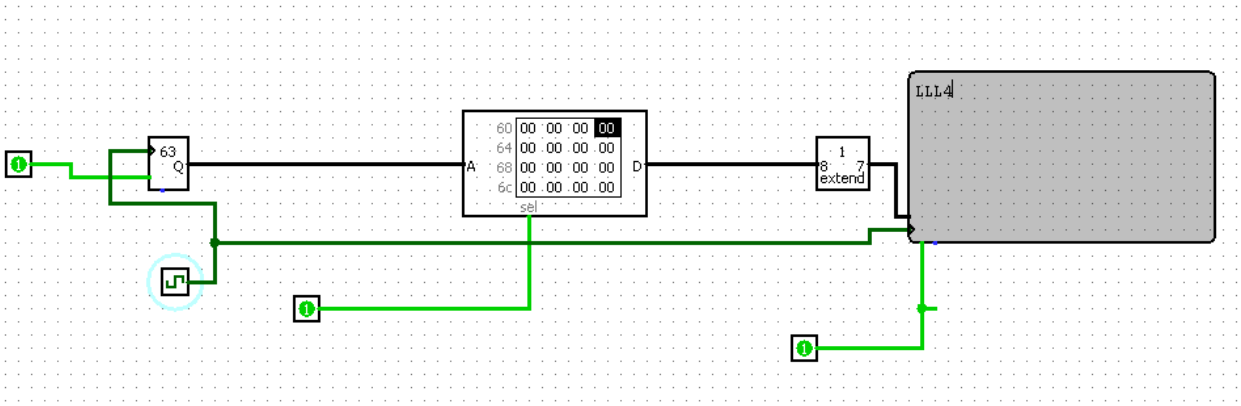


Figure 3.7: 8 Bit ROM in LogiSim

3.2.2.1 PINS

A on west edge (input, bit width matches Address Bit Width attribute)

Selects which of the values are currently being accessed by the circuit.

D on east edge (input/output, bit width matches Data Bit Width attribute)

Outputs the value at the currently selected address at the *D* pin if *sel* is 1 or floating. If *sel* is 0, then *D* will be floating.

sel on south edge (input, bit width 1)

If you have just one ROM module, ignore this input. If you have multiple ROM modules in parallel, you can use this input to enable or disable the entire ROM module, based on whether the value is 1 or 0. In other words, when this is 0, no value is emitted on the *D* output.

3.2.2.2 ATTRIBUTES

Address Bit Width

The bit width of the address bits. The number of values stored in RAM is $2^{addrBitWidth}$.

Data Bit Width

The bit width of each individual value in memory.

Contents

Stores the contents of memory.

3.3 Lab Activities

3.3.1 Task-1: Implement Figure: 3.5 in LogiSim

3.3.2 Task-2 Implement 32 Bit RAM in LogiSim using Random Generator and Counter Components for inputs and Bit Extender and TTY for output.

3.3.3 Task-3 Implement 32 Bit ROM in LogiSim using Random Generator and Counter Components for inputs and Bit Extender and TTY for output.

Lab Exercise and Summary

Summary should cover Introduction, Procedure, Data Analysis and Evaluation.

Student's Signature: _____ **Date: _____**

Cognitive Activity

Q1. A memory block has a 4-bit address bus. How many distinct locations can it address, and why? If you now need to store 64 locations, what is the minimum number of address bits required? **(5)**

Ans: _____

_____

_____

_____

_____

Q2. Explain, step by step, how you would connect a Counter and a Random Number Generator together with a RAM block in LogiSim so that a sequence of memory addresses is automatically filled with random values. **(5)**

Ans: _____

_____

_____

_____

_____

Obtained Marks	**/10**

Psychomotor Activity 1 — Experimental Setup

S. No	Criteria	Performance	Description	Marks
1	Tool Setup (4)	Level 4	Opens and configures LogiSim and selects the required environment correctly and independently.	4
		Level 3	Configures the required tool with minor errors or assistance.	3
		Level 2	Completes the setup with considerable assistance.	2
		Level 1	Setup is incomplete and requires substantial assistance.	1
2	File/Design Setup (4)	Level 4	Correctly creates/selects the required assembly file, Logisim circuit/design and required components for the Logisim RAM/ROM design.	4
		Level 3	File/design setup is mostly correct with minor errors or omissions.	3
		Level 2	Setup is partially completed and requires assistance.	2
		Level 1	Major errors or omissions are present in the setup.	1
3	Parameter Setup (2)	Level 2	Correctly defines required data, registers, parameters, components and initial conditions.	2
		Level 1	Most required inputs/components are correctly configured with minor errors.	1
			Total Obtained	/10

If a student is absent:

Criteria	Description	Marks
Absent	Student is absent from the laboratory activity.	0

Psychomotor Activity 2 — Implementation + Results

S. No	Criteria	Performance	Description	Marks
1	**Implementation (4)**	Level 4	Implements the required Logisim RAM/ROM design correctly and independently.	**4**
		Level 3	Implements the required program/design with minor errors or assistance.	**3**
		Level 2	Partially implements the program/design and requires considerable assistance.	**2**
		Level 1	Implementation is largely incomplete and requires substantial assistance.	**1**
2	**Execution/Simulation (2)**	Level 2	Executes the RISC-V program or simulates the Logisim design correctly and handles basic errors appropriately.	**2**
		Level 1	Executes/simulates the work with minor errors or assistance.	**1**
3	**Results/Output (4)**	Level 4	Obtains correct results and clearly demonstrates the required program output or circuit behavior.	**4**
		Level 3	Obtains mostly correct results with minor errors.	**3**
		Level 2	Obtains partially correct results with noticeable errors or omissions.	**2**
		Level 1	Results are largely incorrect or incomplete.	**1**
			Total Obtained	**/10**

If a student is absent:

Criteria	Description	Marks
Absent	Student is absent from the laboratory activity.	**0**

Affective Activity — Lab Report + Viva Voce

S. No	Criteria	Performance	Description	Marks
1	Lab Report Completeness & Organization (4)	Level 4	Report is complete, well organized and demonstrates full responsibility for the assigned work.	4
		Level 3	Report is complete with minor omissions or organizational issues and demonstrates satisfactory responsibility for the assigned work.	3
		Level 2	Report is partially complete with several omissions and demonstrates limited responsibility for the assigned work.	2
		Level 1	Report has major omissions or poor organization and demonstrates minimal responsibility for the assigned work.	1
2	Code/Design, Results & Conclusion (2)	Level 2	Logisim RAM/ROM design, results, and conclusion are correctly presented and discussed, demonstrating ownership of the assigned work.	2
		Level 1	Logisim RAM/ROM design, results, or conclusion are presented with minor errors or omissions.	1
3	Viva Voce (4)	Level 4	Clearly explains the assigned Logisim RAM/ROM design, working, and results, demonstrating individual responsibility, participation, and effective communication.	4
		Level 3	Explains most of the assigned program/design and results correctly, with minor difficulty, and demonstrates good individual participation.	3
		Level 2	Explains basic aspects of the assigned program/design with some prompting and demonstrates basic participation.	2
		Level 1	Demonstrates limited understanding or involvement and requires substantial prompting to explain the assigned work.	1
			Total Obtained	/10

The student has not submitted the report and has not appeared in the Viva Voce.

Criteria	Description	Marks
Lab Report and Results Not Submitted	Student has not submitted the report and results file.	0
Absent in Viva Voce	Student is absent from the viva voce.	0

Instructor's Signature: _____ **Date: _____**